F81803

Super I/O with Hardware Monitor

FINTEK CONFIDENTIAL

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F81803 Datasheet Revision History

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0.10P	January, 2013	-	Preliminary version
0.11P	March, 2013	-	Add Chapter 4, 5 and 6.

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1 General Description

The F81803 which is the featured IO chip for PC system is equipped with ATX_AT Strapping pin, two UART Ports with up to 128 bytes FIFO, provide 9 bit (multidrop) function, one 80 port (multi with COM2), Hardware Keyboard Controller. The UART supports legacy speeds up to 115.2K bps as well as even higher baud rates of 230K, 460K, or 921K bps to support higher speed modems. The F81803 integrates with hardware monitor, 7 sets of voltage sensor, 2 sets of creative auto-controlling fans and 2 temperature sensor pins for the accurate dual current type temperature measurement for CPU thermal diode or external transistors 2N3906. Others, the F81803 supports newest AMD TSI, Intel PECI 3.0 interfaces and SMBus for temperature sensing and provides the power sequence controller function for AMD platform.

The F81803 provides flexible features for multi-directional application. For instance, the F81803 provides 15 GPIO pins (multi-pin), IRQ sharing function also designed in UART feature for particular usage and accurate current mode H/W monitor will be worth in measurement of temperature, provides 3 modes fan speed control mechanism included Manual Mode/Stage Auto Mode/Linear Auto Mode for users' selection.

In order to save the current consumption when the system is in the soft off state which is so called power saving function. The power saving function supports that system boot-on not only by pressing the power button but also by the wake-up events via RI#. When the system enters the S4/S5 state, F81803 can cut off the VSB power rail which supplies power source to the devices like the LAN chip, the chipset, the SIO, the audio codec, DRAM, and etc. The PC system can be simulated to G3-like state when system enters the S4/S5 states. At the G3-like state, the F81803 consumes the 5VA power rail only. The integrated two control pins are utilized to turn on or off VSB power rail in the G3-like status. The turned on VSB rail is supplied to a wake up device to fulfill a low power consumption system which supports a wake up function.

These features as above description will help you more and improve the product value. The F81803 is powered by 3.3V voltage, with the LPC interface in the green package of 64-TQFP (7mm*7mm).

2 Feature List

- **General Functions**
  - Comply with LPC Spec. 1.1
  - Support DPM (Device Power Management), ACPI
  - Support AMD power sequence controller
  - Provides two UARTs with programmable 16/32/64/128 bytes FIFO
    - ✓ Multi drop function
    - ✓ Support IRQ Sharing function.
    - ✓ Provide auto flow control function
  - Hardware KBC and Parallel Port
  - H/W monitor functions
  - Support AMD TSI, MXM, Intel PECI 3.0 interface
  - Provide SMBus slave & master function
  - Provide 2 sets of SMBus Interface.
  - 15 GPIO Pins for flexible application
  - Provide Power Saving Function (Comply ERP lot 6.0)
  - Support Intel Deep Sleep Well (DSW) Timing Sequence
  - Provide wake-up events via power button, RI#
  - Provide ATX emulates AT function
  - 24/48 MHz clock input
  - Packaged in 64-TQFP and powered by 3.3VCC

- **UART**
  - Two high-speed 16C550/16C650/16C750/16C850 compatible UART with programmable 16/32/64/128 bytes FIFO
  - Baud rate up to 115.2K, max. up to 1.5M
  - Support IRQ sharing
  - Support Ring-In Wakeup
  - Provide auto flow control function
  - Provide Multi drop (9-bits) Function for Gaming Machine
  - Support programmable register for TX/RX only, Mondem control, & fully UART function

- **80-Port Interface**
  - Monitor 0x80 Port and output the value via signals defined for 7-segment display.
  - High nibble and low nibble are outputted interleaved at 1KHz frequency.
  - 80-Port output via COM2 interface.

- Provide MXM/PECI/TSI/T1/T2 value via 80-port

◆ **Hardware Monitor Functions**

- 2 dual current type (±3℃) thermal inputs for CPU thermal diode and 2N3906 transistors
- Temperature range -40℃~127℃
- 7 sets voltage monitoring (2 external and 5 internal powers)
- Voltage monitor supports Over/Under Voltage Protection (OVP/UVP)
- High limit signal (PME#) for Vcore level
- 2 fan speed monitoring inputs
- 2 fan speed PWM/DC control outputs(support 3 wire and 4 wire fans)
- The Fan PWM output frequency can be programmed as 23.5/11.75/5.875KHz, & 200Hz for LCD backlight adjustment
- Stage auto mode (4-Limit and 5-Stage)/Linear auto mode/Manual mode
- OVT# hardware signals output
- Case open detection (assert via PME#/BEEP)
- WATCHDOG comparison of all monitored values
- PSIN# detection time flag is programmable 1s(default)/2s/3s/4s (Usage: Enter BIOS setting page under the quick booting WIN 8 OS)

◆ **Keyboard Controller**

- LPC interface support serial interrupt channel 1, 12.
- Two 16bit Programmable Address fully decoder, default 0x60 and 0x64.
- Support two PS/2 interface, one for PS/2 mouse and the other for keyboard.
- Programmable compatibility with the 8042.
- Support both interrupt and polling modes.
- Fast Gate A20 and Hardware Keyboard Reset.

◆ **Power Saving Controller**

- ACPI Timing and Power Control
- Wake-up Supported
- G3-like Timing Control
- Comply With ERP Lot 6.0
- Built in Soft Start Function for Two Control Pins with VSB Power Sources Control.
- Event in input via GPIo05~06, GPIO16 , GPIO44~47, RI# pins

◆ **GPIO Function**

- Total 15 pins GPIO

- GPIO0X could be reset by 3VA/VBAT via the register setting
- GPIO05, GPIO06, GPIO16 support SMI event via PME# or SIRQ
- Scan Code
  - ✧ Support Scan Code Via GPIO2x
  - ✧ GPIO24~27 support programmable combination keys (single or dual code Clt+Alt+code)
- All GPIO supports digit IO for Input/Output control, Output data control, input status.
- Support High/Low Level/Pulse, Open Drain/Push Pull function selection

◆ **Watch Dog Timer**

- Time resolution minute/second
- Maximum 256 minutes or 256 seconds
- Output signal via WDTRST#/PWOK
- WDT could also wake up via PME#, PSOUT#
- Provide hardware strapping pin & auto reload function

◆ **Integrate Intel PECI 3.0 Spec.**

◆ **Integrate Intel Cougar Point Timing/DSW Timing**

◆ **Support AMD Power Sequence Controller**

◆ **Intel Block Read/Write SMBus Interface**

◆ **Provide ATX Emulates AT Function**

◆ **AMD TSI/MXM/I2C Interface**

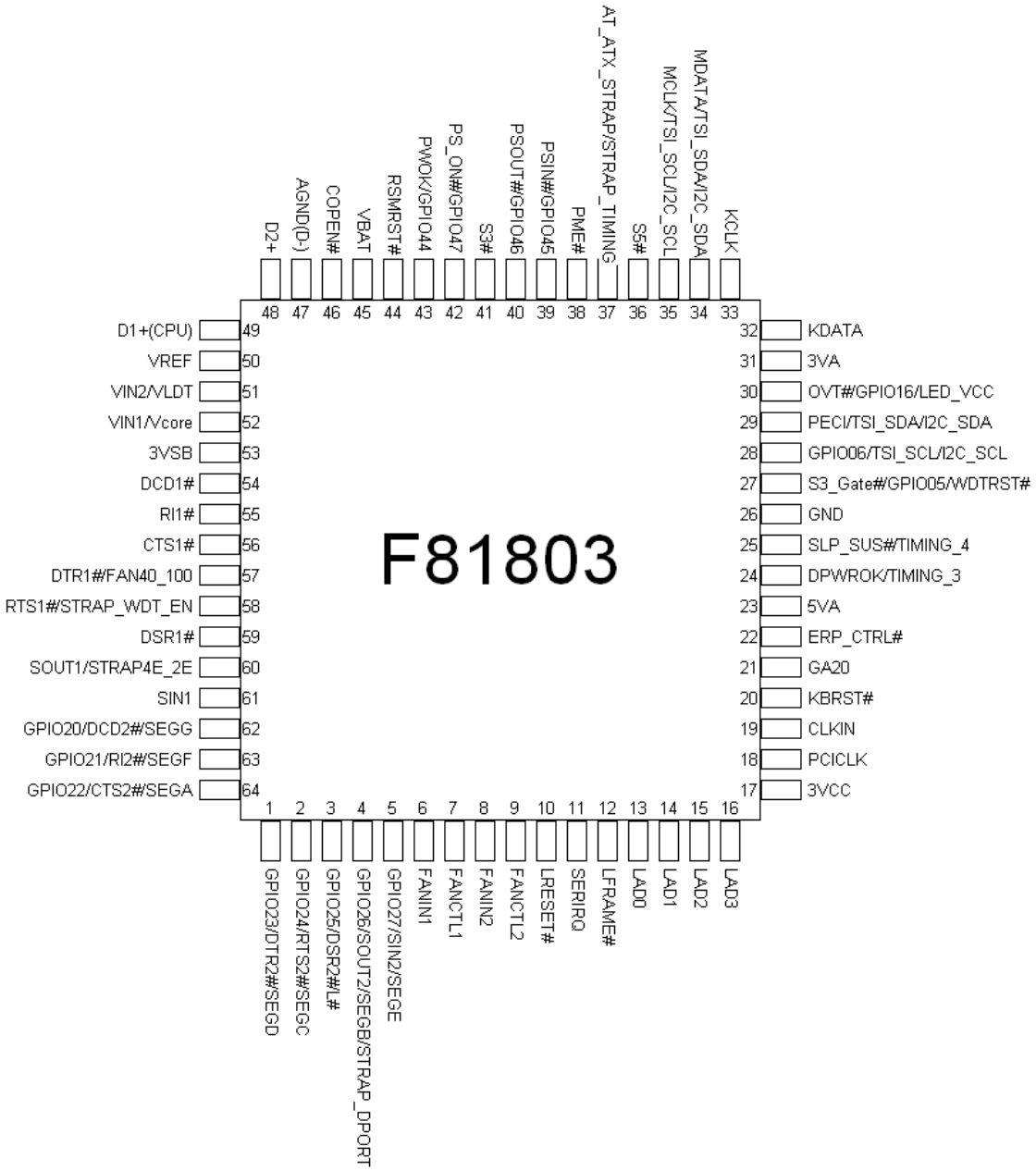
- Support slave interface to report the hardware monitor data under S0/S3/S5
- I2C slave default address is 5Ch
- Support master interface to get the thermal data via PCH & MXM module
- Provide 2 sets of SMBus for TSI/MXM/I2C interface.
- AMD TSI/MXM/I2C interfaces could be selected individually via 2 sets of pins → pin 28 (GPIO06/TSI_SCL/I2C_SCL), & pin 29(PECI/TSI_SDA/I2C_SDA); pin 34 (MDATA/TSI_SDA/I2C_SDA), & pin 35 (MCLK/TSI_SCL/I2C_SCL).

◆ **Package**

- 64-TQFP (7*7) Green Package

3 Pin Configuration

Figure1. F81803 pin configuration (7*7)



4 Pin Description

4.1 Power Pins

Pin No.	Pin Name	Type	Description
17	3VCC	P	Power supply voltage input with 3.3V. This pin support OVP/UVP function, and default is disabled.
23	5VA	P	5V standby power input (via ATX Power). Provide 5VA voltage detection & power good signal for DPWOK function. This power only for power sequence use.
31	3VA	P	3.3V standby power input (via ATX Power). Provide 3VA voltage detection & power good signal for DPWOK function.
45	VBAT	P	Battery voltage input where power good level is 2.0V. Provide VBAT detection function.
47	AGND(D-)	P	Analog GND
53	3VSB	P	Analog Stand-by power supply voltage input 3.3V.
26	GND	P	Digital GND

4.2 LPC Interface

Pin No.	Pin Name	Type	PWR	Description
10	LRESET#	$IN_{st,5v}$	3VCC	Reset signal. It can connect to PCIRST# signal on the host.
11	SERIRQ	$I/O_{16t,u47k}$	3VCC	Serial IRQ input/Output.
12	LFRAME#	$IN_{st,u47k}$	3VCC	Indicates start of a new cycle or termination of a broken cycle.
13-16	LAD[0:3]	$I/O_{16t,u47k}$	3VCC	These signal lines communicate address, control, and data information over the LPC bus between a host and a peripheral.
18	PCICLK	$IN_{st,5v}$	3VCC	33MHz PCI clock input.

4.3 System Clock Input

Pin No.	Pin Name	Type	PWR	Description
19	CLKIN	$IN_{st,5v}$	3VCC	System clock input. According to the input frequency 24/48MHz.

4.4 UART & Debug Port

Pin No.	Pin Name	Type	PWR	Description
54	DCD1#	$IN_{st,5v}$	3VCC	Data Carrier Detect. An active low signal indicates the modem or data set has detected a data carrier.
55	RI1#	$IN_{st,5v}$	I_VSB3V	Ring Indicator. An active low signal indicates that a ring signal is being received from the modem or data set.
56	CTS1#	$IN_{st,5v}$	3VCC	Clear To Send is the modem control input.
57	DTR1#	$O_{8t,5v,u47k}$	3VCC	UART 1 Data Terminal Ready. An active low signal informs the modem or data set that controller is ready to communicate. Internal 47k ohms pulled high and disable after power on strapping.
	FAN40_100	IN_{t5v}		Power on strapping pin: 1(Default): (Internal pull high) Power on fan speed default duty is 40%.(PWM) 0: (External pull down) Power on fan speed default duty is 100%.(PWM)
58	RTS1#	$O_{8t,5v,u47k}$	3VCC	UART 1 Request To Send. An active low signal informs the modem or data set that the controller is ready to send data.
	STRAP_WDT_EN	IN_{t5v}		Power on strapping: (Internal pull high) 1 (Default):Disable WDT 0 :Enable WDT
59	DSR1#	$IN_{st,5v}$	3VCC	Data Set Ready. An active low signal indicates the modem or data set is ready to establish a communication link and transfer data to the UART.
60	SOUT1	$O_{8t,5v,u47k}$	3VCC	UART 1 Serial Output. Used to transmit serial data out to the communication link. Internal 47k ohms pulled high and disable after power on strapping.
	STRAP4E_2E	IN_{t5v}		Power on strapping: 1(Default): Configuration register 4E 0: Configuration register 2E
61	SIN1	$IN_{st,5v}$	3VCC	Serial Input. Used to receive serial data through the communication link.
62	GPIO20	$I/OOD_{8st,5v}$	3VCC	Default General Purpose IO.
	DCD2#	$IN_{st,5v}$		Data Carrier Detect. An active low signal indicates the modem or data set has detected a data carrier. The function is selected by register setting.
	SEGG	O_{18}		SEGG for 7-segment display. (Select by pin 5 power on strapping)
63	GPIO21	$I/OOD_{8st,5v}$	3VCC	Default General Purpose IO.
	RI2#	$IN_{st,5v}$		Ring Indicator. An active low signal indicates that a ring signal is being received from the modem or data set.

				The function is selected by register setting.
	SEGF	O_{18}		SEGF for 7-segment display. (Select by pin 5 power on strapping)
64	GPIO22	$I/OOD_{8st,5v}$	3VCC	Default General Purpose IO.
	CTS2#	$IN_{st,5v}$		Clear To Send is the modem control input. The function is selected by register setting.
	SEGA	O_{18}		SEGA for 7-segment display. (Select by pin 4 power on strapping)
1	GPIO23	$I/OOD_{8st,5v}$	3VCC	Default General Purpose IO.
	DTR2#	$O_{8t,5v,u47k}$		UART 2 Data Terminal Ready. An active low signal informs the modem or data set that controller is ready to communicate. The function is selected by register setting.
	SEGD	O_{18}		SEGD for 7-segment display. (Select by pin 5 power on strapping)
2	GPIO24	$I/OOD_{8st,5v}$	3VCC	Default General Purpose IO.
	RTS2#	$O_{8t,5v,u47k}$		UART 2 Request To Send. An active low signal informs the modem or data set that the controller is ready to send data. The function is selected by register setting.
	SEGC	O_{18}		SEGC for 7-segment display. (Select by pin 5 power on strapping)
3	GPIO25	$I/OOD_{8st,5v}$	3VCC	Default General Purpose IO.
	DSR2#	$IN_{st,5v}$		Data Set Ready. An active low signal indicates the modem or data set is ready to establish a communication link and transfer data to the UART. The function is selected by register setting.
	L#	O_{30}		L# for 7-segment display. (Select by pin 5 power on strapping)
4	GPIO26	$I/OOD_{8st,5v}$	3VCC	Default General Purpose IO.
	SOUT2	$O_{8t,5v,u47k}$		UART 2 Serial Output. Used to transmit serial data out to the communication link. The function is selected by register setting.
	SEGB	O_{18}		SEGB for 7-segment display. (Select by pin 5 power on strapping)
	STRAP_DPORT	IN_{t5v}		Strap for 80 Port. Default internal Pull High for 80 Port Enable.
5	GPIO27	$I/OOD_{8st,5v}$	3VCC	Default General Purpose IO.
	SIN2	$IN_{st,5v}$		Serial Input. Used to receive serial data through the communication link. The function is selected by register setting.
	SEGE	O_{18}		SEGE for 7-segment display. (Select by pin 5 power on strapping)

4.5 Hardware Monitor

Pin No.	Pin Name	Type	PWR	Description
51	VIN2/VLDT	AIN	3VSB	Voltage input 2 or VLDT input used in AMD platform. The input voltage level for timing control usage must be over 1V after voltage divider.
52	VIN1/Vcore	AIN	3VSB	Voltage Input for Vcore. The input voltage level for timing control usage must be over 0.7V.
6	FANIN1	$IN_{st,5v}$	3VCC	Fan 1 tachometer input.
7	FANCTL1	$OOD_{12,5v}$ AOUT	3VCC	Fan 1 control output. It is also a trap pin to select a PWM or a DAC output, except being an output pin. It defaults to be a voltage output by pulling down 100k internally. It is set as a PWM output as connected a 4.7K resistor and pulled high to 3.3V. The PWM output frequency can be programmed to 220Hz for LCD backlight control.
8	FANIN2	$IN_{st,5v}$	3VCC	Fan 2 tachometer input.
9	FANCTL2	$OOD_{12,5v}$ AOUT	3VCC	Fan 2 control output. It is also a trap pin to select a PWM or a DAC output, except being an output pin. It defaults to be a voltage output by pulling down 100k internally. It is set as a PWM output as connected a 4.7K resistor and pulled high to 3.3V. The PWM output frequency can be programmed to 220Hz for LCD backlight control.
28	GPIO06	$I/OOD_{12st,5v}$	3VSB	General Purpose IO.
	TSI_SCL	$OD_{12st,5v}$		Clock output for AMD TSI.
	I2C_SCL	$I_{LV}/OD_{12st,5v}$		SMBUS Interface CLOCK pin.
29	PECI	$I_{LV}/O_{D8,S1}$	3VSB	Intel PECI hardware monitor interface. When TIMING_GPIO pin is set in GPIO function (INTEL mode). PECI function can be set by the register.
	TSI_SDA	$I_{LV}/OD_{12st,5v}$		AMD TSI Interface DATA pin.
	I2C_SDA	$I_{LV}/OD_{12st,5v}$		SMBUS Interface DATA pin.
30	OVT#	$OD_{12,5v}$	3VSB	Over temperature signal output.
	GPIO16	$I/OOD_{12st,5v}$		General Purpose IO.
	LED_VCC	$OD_{12,5v}$		Power LED for VCC. This function is selected by the register setting.
38	PME#	$OD_{12,5v}$	3VSB	Generated PME event. It supports the PCI PME# interface. This signal allows the peripheral to request the system to wake up from the S3 state.
48	D2+	AIN	3VSB	Thermal diode/transistor temperature sensor input.
49	D1+(CPU)	AIN	3VSB	CPU thermal diode/transistor temperature sensor input. This pin is for CPU use.
50	VREF	AOUT	3VSB	Voltage sensor output.

4.6 KBC Function

Pin No.	Pin Name	Type	PWR	Description
20	KBRST#	$OD_{16,5v,u10k}$	3VCC	Keyboard reset. This pin is high after system reset. Internal pull high 3.3V with 10k ohms. (KBC P20)
21	GA20	$OD_{16,5v,u10k}$	3VCC	Gate A20 output. This pin is high after system reset. Internal pull high 3.3V with 10k ohms. (KBC P21)
32	KDATA	$I/OD_{16st,5V}$	3VSB	Keyboard Data.
33	KCLK	$I/OD_{16st,5V}$	3VSB	Keyboard Clock.
34	MDATA	$I/OD_{16st,5V}$	3VSB	PS2 Mouse Data.
	TSI_SDA	$I_{LV}/OD_{12st,5v}$		AMD TSI Interface DATA pin.
	I2C_SDA	$I_{LV}/OD_{12st,5v}$		SMBUS Interface DATA pin.
35	MCLK	$I/OD_{16st,5V}$	3VSB	PS2 Mouse Clock.
	TSI_SCL	$OD_{12st,5v}$		Clock output for AMD TSI.
	I2C_SCL	$I_{LV}/OD_{12st,5v}$		SMBUS Interface CLOCK pin.

4.7 ACPI Function Pins

Pin No.	Pin Name	Type	PWR	Description
36	S5#	$IN_{st,5v}$	3VSB	S5# signal input.
37	AT_ATX_STRAP	$IN_{t,5v}$	3VSB	Power on trapping: 1: ATX mode (Default, internal pull high 47k Ω). 0: AT mode. The external resisters are necessary to decide the mode. The mode is strapped at 16ms after 3VA & 5VA power good level. Check the power on strapping section for the detail.
	STRAP_TIMING	$IN_{st,5v}$		Strap Pin for AMD and Intel Cougar Point timing. Internal pull high with AMD timing (Default). The external resisters are necessary to decide the mode. The mode is strapped at 16ms after 3VA & 5VA power good level. Check the power on strapping section for the detail.
39	PSIN#	$IN_{st,5v}$	3VSB	Main power switch button input.
	GPIO45	$I/OOD_{12st,5v}$		General Purpose IO.
40	PSOUT#	$OD_{12,5v}$	3VSB	Panel Switch Output. This pin is low active and pulse output. It is power on request output#.
	GPIO46	$I/OOD_{12st,5v}$		General Purpose IO.
41	S3#	$IN_{st,5v}$	3VSB	S3# Input is Main power on-off switch input.
42	PS_ON#	$OD_{12,5v}$	3VSB	Power supply on-off control output. Connect to ATX power supply PS_ON# signal.
	GPIO47	$I/OOD_{12st,5v}$		General Purpose IO.
43	PWOK	$OD_{12,5v}$	VBAT	PWOK function, It is power good signal of VCC, which is

				delayed 400ms (default) as VCC arrives at 2.8V. The additional PWOK delay is programmable 100ms/200ms (Default)/400ms.
	GPIO44	$I/OOD_{12st,5v}$		General Purpose IO.
44	RSMRST#	$OD_{12,5v,u10k}$	VBAT	Resume Reset# function, It is power good signal of VSB, which rises delayed 66ms as VSB arrives at 2.8V and falls as VSB drops to 2.6V. There is an option to set RSMRST# rises at 3.05V and falls at 2.95V.
46	COPEN#	$IN_{st,5v}$	VBAT	Case Open Detection #. This pin is connected to a specially designed low power CMOS flip-flop backed by the battery for case open state preservation during power loss.

4.8 Power Saving and Others

Pin No.	Pin Name	Type	PWR	Description
22	ERP_CTRL#	OD_{12}	3VSB	Standby power rail control pin. This pin controls an external PMOS to turn on or off the standby power rail. In the S5 state, the default is set to 1 to cut off the standby power rail.
24	DPWOK	$OD_{12,5v}$	3VSB	Resume Reset# function, It is power good signal of VSB, which is delayed 66ms as VSB arrives at 4.4V. Couple this pin to PCH when system supports Intel DSW state function.
	TIMING_3	$OD_{12,5v}$		Active high. Timing sequence 3 of power on/off sequence pins. The external pull high resistor is required. (Detected by VIN3 level good)
25	SLP_SUS#	$IN_{st,lv}$	3VSB	For Intel CPT DSW function. Connect to PCH SLP_SUS pin.
	TIMING_4	$OD_{12,5v}$		Active high. Timing sequence 4 of power on/off sequence pins. The external pull high resistor is required. (Detected by VIN1 level good)
27	S_3_Gate#	OD_{12}	3VSB	Status Pin1 for S0#/S3#/S5# states application. (Default function) In S0# → S_3_Gate# pin status is Tri-state. In S3# → S_3_Gate# pin status is Low level. In S5# → S_3_Gate# pin status is Tri-state.
	GPIO05	$I/OOD_{12st,5v}$		General Purpose IO. GPIO function is selected by register setting
	WDTRST#	$OD_{12,5v}$		Watch dog timer signal output. WDT could be asserted via WDTRST#/PWOK.

5 Function Description

5.1 Power on Strapping Option

The F81803 provides seven pins for power on hardware strapping to select functions. There is a form to describe how to set the functions you want.

Table1: Power on trap configuration

<table>
<tr><th>Pin No.</th><th>Symbol</th><th>Value</th><th>Description</th></tr>
<tr><td rowspan="2">4</td><td rowspan="2">STRAP_DPORT</td><td>1</td><td>Enable 80 Port (Default)</td></tr>
<tr><td>0</td><td>Disable 80 Port</td></tr>
<tr><td rowspan="2">7</td><td rowspan="2">FANCTL1</td><td>1</td><td>FANCTRL1 is PWM mode. Connect a 4.7K resistor and pull high to 3.3V.</td></tr>
<tr><td>0</td><td>FANCTLR1 is DAC mode. (Default)</td></tr>
<tr><td rowspan="2">9</td><td rowspan="2">FANCTL2</td><td>1</td><td>FANCTRL2 is PWM mode. Connect a 4.7K resistor and pull high to 3.3V.</td></tr>
<tr><td>0</td><td>FANCTLR2 is DAC mode. (Default)</td></tr>
<tr><td rowspan="2">57</td><td rowspan="2">FAN40_100</td><td>1</td><td>Power on Fan speed default duty is 40% (PWM) (Default)</td></tr>
<tr><td>0</td><td>Power on Fan speed default duty is 100%(PWM)</td></tr>
<tr><td rowspan="2">58</td><td rowspan="2">STRAP_WDT_EN</td><td>1</td><td>Disable WDT after power on (Default).</td></tr>
<tr><td>0</td><td>Enable WDT after power on.</td></tr>
<tr><td rowspan="2">60</td><td rowspan="2">STRAP4E_2E</td><td>1</td><td>Configuration Register I/O port is 4E/4F. (Default)</td></tr>
<tr><td>0</td><td>Configuration Register I/O port is 2E/2F.</td></tr>
<tr><td>37</td><td>STRAP_TIMING
AT_ATX_STRAP</td><td>-</td><td>This pin is used to determine TIMING_EN and AT_ATX_MODE register (Port Select Register — Index 27h [1-0]) power on strap value. No internal pull up/down reisister is built in, so the external resistors are needed. Refer to following table:
<table>
<tr><th>Condition</th><th>TIMING_EN</th><th>AT_ATX_MODE</th></tr>
<tr><td>0/8*3VA</td><td>0 (Disable)</td><td>0 (ATX)</td></tr>
<tr><td>3/8*3VA</td><td>0 (Disable)</td><td>1 (AT)</td></tr>
<tr><td>5/8*3VA</td><td>1 (Enable)</td><td>0 (ATX)</td></tr>
<tr><td>7/8*3VA</td><td>1 (Enable)</td><td>1 (AT)</td></tr>
</table>
</td></tr>
</table>

5.2 Hardware Monitor - Voltage

For the 8-bit ADC has the 8mv LSB, the maximum input voltage of the analog pin is 2.048V. Therefore the voltage under 2.048V (ex: 1.5V) can be directly connected to these analog inputs. The voltage higher than 2.048V should be reduced by a factor with external resistors so as to obtain the input range. Only 3VCC/3VSB/VBAT is an exception for it is main power of the F81803. Therefore 3VCC/3VSB/VBAT can directly connect to this chip's power pin and need no external resistors. There are two functions in this pin with 3.3V. The first function is to supply internal analog power of the F81803 and the second function is that voltage with 3.3V is connected to internal serial resistors to monitor the +3.3V voltage. The internal serial resistors are two 150K ohm, so that the internal reduced voltage is half of +3.3V.

There are four voltage inputs in the F81803 and the voltage divided formula is shown as follows:

$$VIN = V_{+12V} \times \frac{R_2}{R_1 + R_2}$$

Where V_{+12v} is the analog input voltage, for example:

If we choose R1=27K, R2=5.1K, the exact input voltage for V+12v will be 1.907V, which is within the tolerance. As for application circuit, it can be refer to the figure shown as follows.

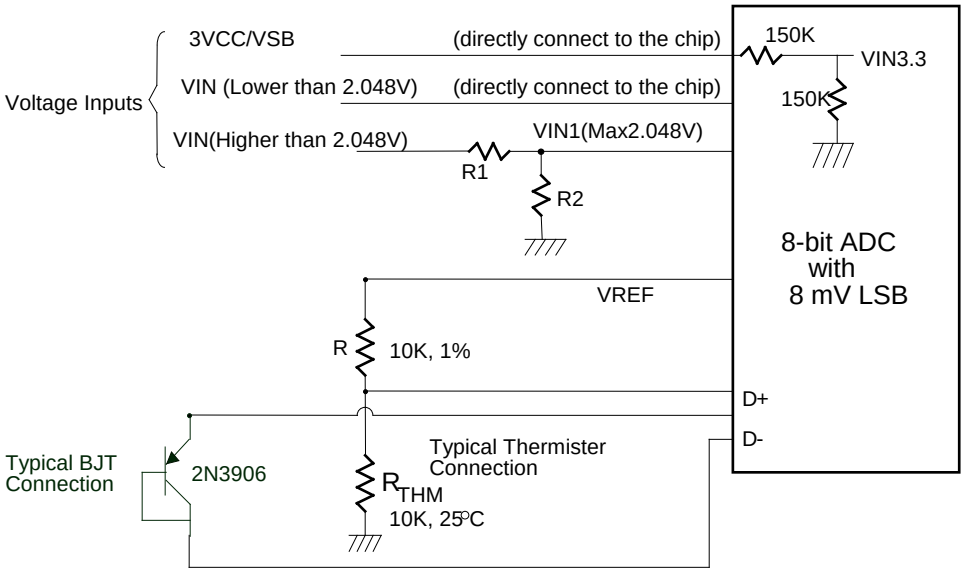


Figure 2. Hardware monitor configuration

5.2.1 Over Voltage & Under Voltage Protection

F81803's **VCC (Only)** could protect the damage from voltage spikes via over voltage & under voltage protection (OVP & UVP) function. Voltage protection function is enabled via setting the related register. When force mode occurs, the system would shut down and the system cannot be re-booted at all. Only re-plugging the power code (cut off VSB) could re-activate or re-boot the system under force mode.

5.2.2 ADC Noise Filtering

The ADC is integrating type with inherently good noise rejection. Micro-power operation places constraints on high-frequency noise rejection; therefore, careful PCB board layout and suitable external filtering are required for high-accuracy remote measurement in electronically noisy environment. High frequency EMI is best filtered at D+ and D- with an external 2200pF capacitor. Too high capacitance may introduce errors due to the rise time of the switched current source. Nearly all noise sources tested cause the ADC measurement to be higher than the actual temperature, depending on the frequency and amplitude.

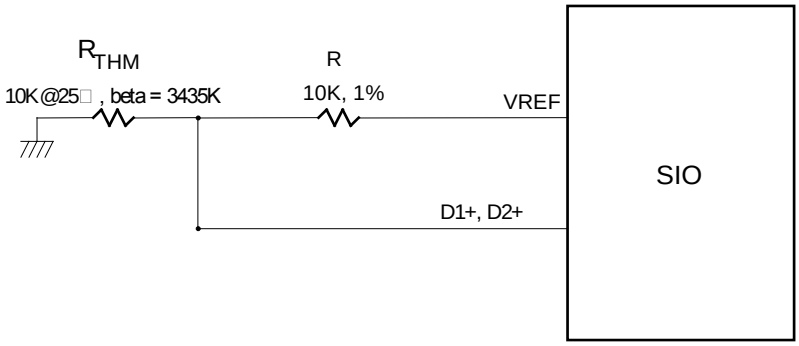
5.3 Hardware Monitor - Temperautre

5.3.1 Monitor Temperature Source

5.3.1.1 Thermistor

F81803 can connect three thermistors to measure environment temperature or remote temperature. The specification of thermistor should be considered to (1) ß value is 3435K (2) resistor value is 10K ohm at 25ºC. In the Figure 3, the thermistor is connected by a serial resistor with 10K ohm, then being connected to VREF.

Figure 3 Hardware monitor configuration



5.3.1.2 Thermal Diode

Also, if the CPU, GPU or external circuits provide thermal diode for temperature measurement, F81803 is capable to these situations. The build-in reference table is for PNP 2N3906 transistor from Table 5-2. In the Figure below, the transistor is directly connected into temperature pins.

Figure 4 Hardware monitor configuration



Table 5-1 Remote-sensor transistor manufacturers

Manufacturer	Model Number
Panasonic	2SB0709 2N3906
Philips	PMBT3906

5.3.1.3 Temperature Monitor

The F81803 monitors three remote temperature sensors. These sensors can be measured from -40°C to 127°C. More detail please refer register description.

Table 2. Display range is from -40°C to 127°C in 2's complement format.

Temperature	Digital Output
-40°C	1101 1000
-1°C	1111 1111
1°C	0000 0001
90°C	0101 1010
127°C	1111 1111
Open	1000 0000

5.3.1.4 Intel PECI

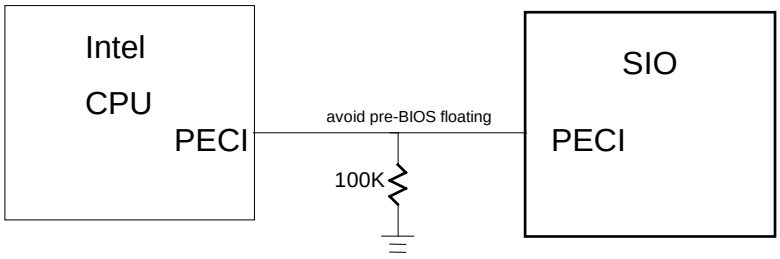
F81803 support Intel PECI1.1/PECI3.0/PECI_Request/PECI_Available interfaces to read temperature from PECI device.

The Platform Environment Control Interface (PECI) uses a single wire for self-clocking and data transfer. The bus requires no additional control lines. The physical layer is a self-clocked on-wire bus that begins each bit with a driven, rising edge from an idle level near zero volts. The duration of the signal driven high depends on whether the bit value is a logic '0' or login '1'. PECI also includes variable data transfer rate established with every message. In this way, it is highly flexible even though underlying logic is simple.

The interface design was optimized for interfacing to Intel processor and chipset components in both single processor and multiple processor environments. The single wire interface provides low board routing overhead for the multiple load connections in the congested routing area near the processor and chipset components. Bus speed, error checking, and low protocol overhead provides adequate link bandwidth and reliability to transfer critical device operating conditions and configuration information.

F81803 can connect to CPU & read the temperature data from CPU directly. Then the fan control machine ofF81803 can implement the fan to cool down CPU temperature. The application circuit is as below.

Figure 5 INTEL PECI Typical Application



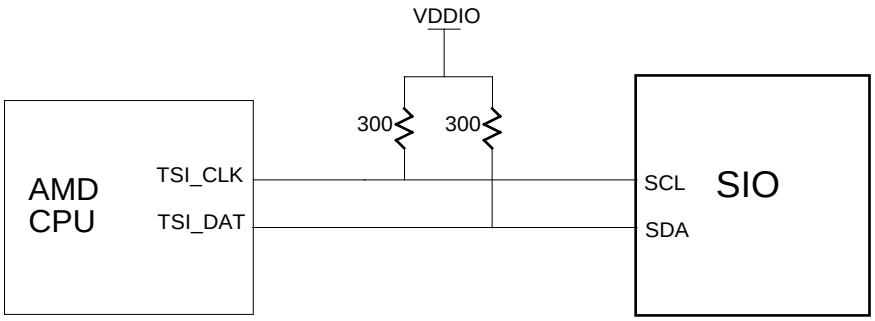
The F81803 integrated most of PECI 3.0 commands for the future advantage application. More detail, please refer to the register descriptions.

5.3.1.5 AMD TSI

TheF81803 provides AMD Temperature Sensor Interface (TSI) interfaces for new generational CPU temperature sensing. In this interface, there are SIC and SID signals for temperature information reading from AMD CPU. The SIC signal is for clocking use, the other is for data transferring. More detail, please refer register description.

The TSI is a simple SMBUS master to communicate with AMD CPU or Intel CPU to getting the temperature of CPU. It supports byte sending, byte reveiving, read/write byte, read/write block and quick command of SMBus protocol. When power on the hardware automatically fetch the temperature use the protocol per the specification of AMD/Intel. User can use the provided registers to control the SCL/SDA as a SMBus master. The SCL signal is for clocking use, the SDA is for data transferring.

Figure 6 AMD TSI typical applications



5.3.2 Temperature Interrupt Detection

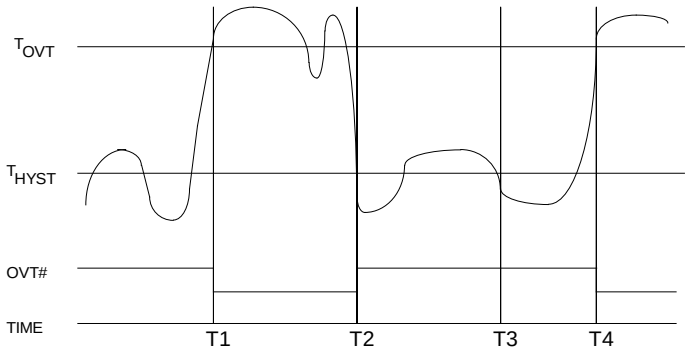
5.3.2.1 Over Temperature Signal (OVT#)

There is a hysteresis mode of OVT# functions, and refers t1 to t4 temperature in Figure 7 Sensor ($\mathbf{T_{OVT}}$) detects temperature exceeds the high threshold limit value and triggers the OVT# when time arrives t1. Time t2, OVT# be asserted until the temperature goes below the hysteresis temperature ($\mathbf{T_{HYST}}$).

Figure 7 Temperature OVT# Signal

T_{OVT} : OVER Temperature Threshold

T_{HYST}: Hysteresis Temperature



5.3.2.2 Power Management Event (PME#)

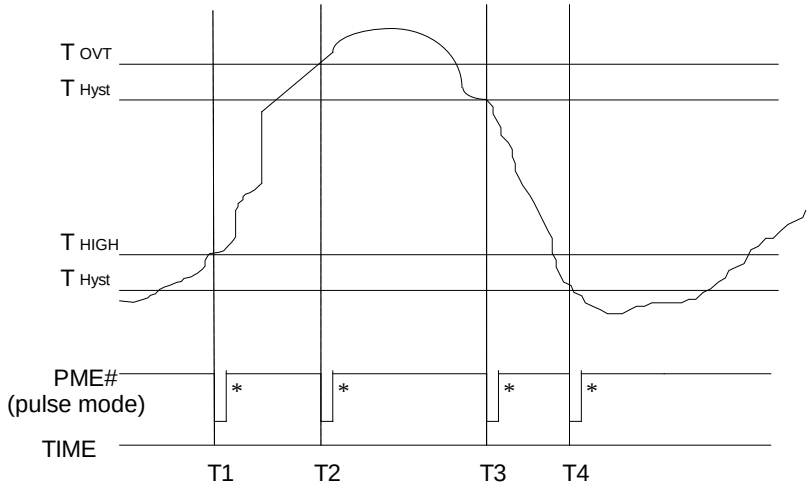
Power Management Event (PME#) interrupt for temperature is shown as Figure 8. Temperature exceeding **T_{HIGH}** (High Limit Threshold) and **T_{OVT}** (OVT Threshold), or going below **T_{HYST}** (High Hysteresis and Low Hysteresis) will cause an interrupt if the previous interrupt has been reset by writing "1" all the interrupt Status Register.

Figure 8 Hysteresis mode illustrations

T_{OVT}: *Over Temperature Threshold*

T_{HYST}: *Hysteresis Temperature*

T_{HIGH}: *High Limit Threshold*



*Interrupt Reset when Interrupt Status Registers are written

5.4 Hardware Monitor - Fan

5.4.1 Fan Speed Count

Inputs are provided by the signals from fans equipped with tachometer outputs. The level of these signals should be set to TTL level, and maximum input voltage cannot be over 5V. If the input signals from the tachometer outputs are over the 5V, the external trimming circuit should be added to reduce the voltage to obtain the input specification.

Determine the fan counter according to:

$$Count = \frac{1.5 \times 10^6}{RPM}$$

In other words, the fan speed counter has been read from register, the fan speed can be evaluated by the following equation. As for fan, it would be best to use 2 pulses tachometer output per round.

$$RPM = \frac{1.5 \times 10^6}{Count}$$

As the register description of datasheet, the parameter “Count” register provides 12-bit resolution for RPM counting. In Fintek design, the value of parameter “Count” is from 4096 ~ 64 (5 bit filter). Therefore the RPM measure capability is from 366 ~ 23438 rpm.
Above example is for 2 pulses tachometer (Normal 4 Phases fan) output per round. If you use 8 Phases fan, means output 4 pulses per round. The RPM measure capability is from 183 ~ 11719 rpm.

5.4.2 Fan Speed Control

The F81803 provides 2 fan speed control methods: one is DAC FAN control and the other is PWM duty cycle.

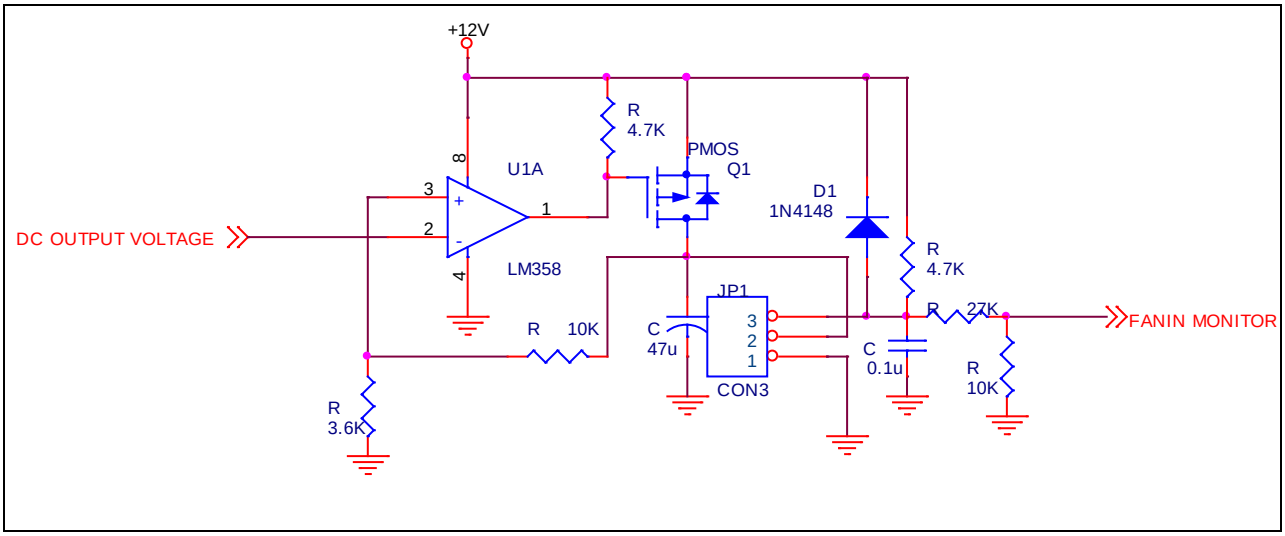
5.4.2.1 DAC Fan Control

The range of DC output is 0~3.3V, controlled by 8-bit register. 1 LSB is about 0.013V. The output DC voltage is amplified by external OP circuit, thus to reach maximum FAN OPERATION VOLTAGE, 12V. The output voltage will be given as followed:

$$\text{Output_voltage (V)} = 3.3 \times \frac{\text{Programmed 8bit Register Value}}{255}$$

And the suggested application circuit for DAC fan control would be:

Figure 9 DAC fan control application circuit

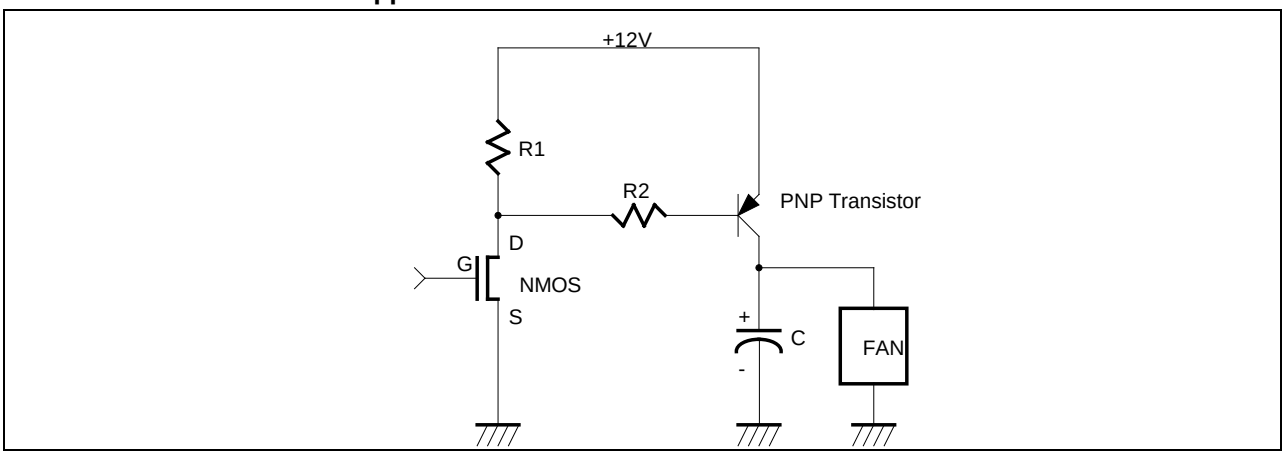


5.4.2.2 PWM duty Fan Control

The duty cycle of PWM can be programmed by a 8-bit register. The default duty cycle is set to 100%, that is, the default 8-bit registers is set to FFh. The expression of duty can be represented as follows.

$$\text{Duty_cycle}(\%) = \frac{\text{Programmed 8bit Register Value}}{255} \times 100\%$$

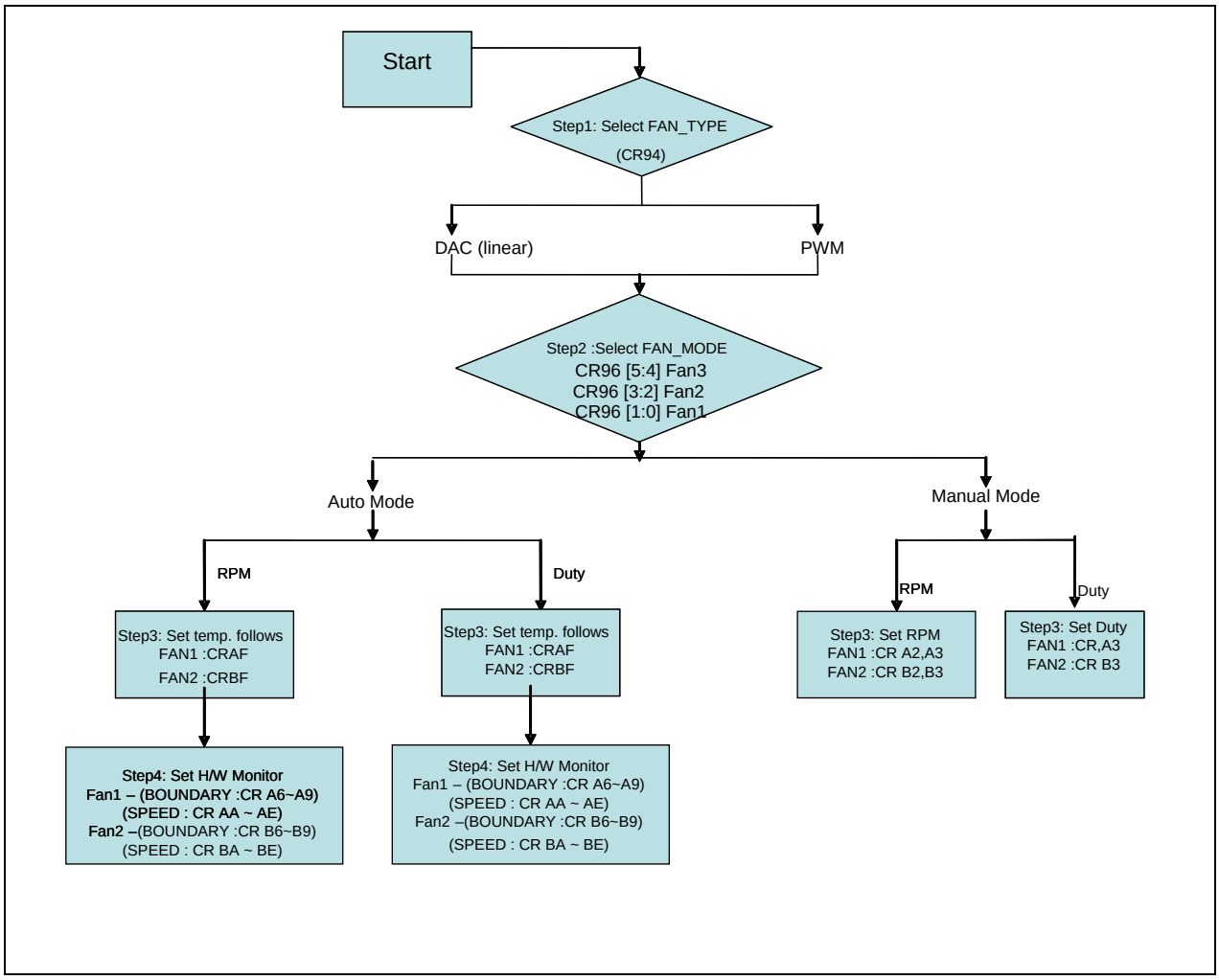
Figure 10 +12/5V PWM fan control application circuit



5.4.3 Fan Speed Control Mechanism

There are some modes to control fan speed and they are 1.Manual mode, 2.Stage auto mode 3. Linear auto mode. Please refer to the figure below. For more detail, please refer the description of registers.

Figure 11 Fan type and mode selection flow



5.4.3.1 Manual mode

For manual mode, it generally acts as software fan speed control.

5.4.3.2 Auto mode

In auto mode, the F81803 provides automatic fan speed control related to temperature variation of CPU/GPU or the system. The F81803 can provide four temperature boundaries and five intervals, and each interval has its related fan speed count. All these values should be set by BIOS first. Take FAN1 for example, the 4 temperature boundaries could be set from register 0xA6 to 0xA9 and the five intervals for fan speed control could be set from register 0xAA to 0xAE. And the hysteresis setting (0 ~ 15°C) could also be found in register 0x98.

The Manual Mode and Auto Mode could be selected by register 0x96h.

There are two kinds of auto mode: stage auto mode and linear auto mode. The “FAN1_ INTERPOLATION_EN” in register 0xAFh is used for linear auto mode enable. The following examples explain the differences for stage auto mode and linear auto mode.

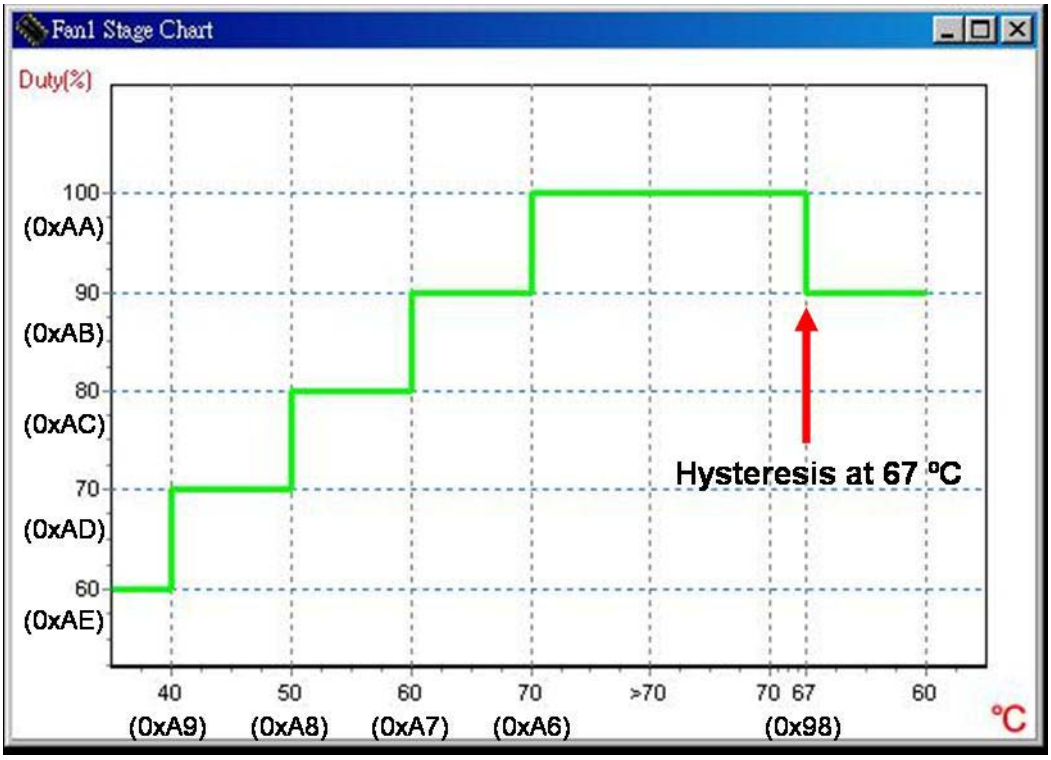
5.4.3.3 Stage auto mode

In this mode, the fan keeps in a same speed for each temperature interval. And there are two types of fan speed setting: PWM Duty and RPM %.

A. Stage auto mode (PWM Duty)

Set the temperature limits as 70°C, 60°C, 50°C, 40°C and the duty as 100%, 90%, 80%, 70%, 60%

Figure 12 Stage mode fan control illustration

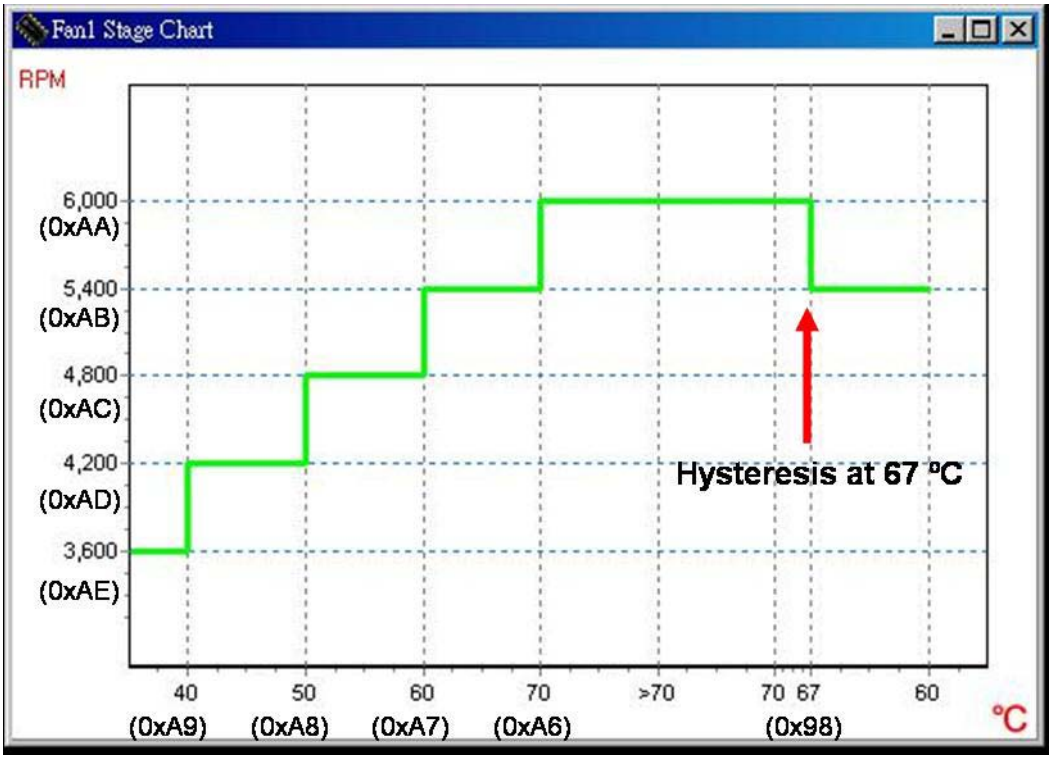


a. Once the temperature is under 40°C, the lowest fan speed keeps in the 60% PWM duty.
b. Once the temperature is over 40°C, 50°Cand 60°C, the fan speed will vary from 70%, 80% to 90% PWM duty and increasing with the temperature level.
c. For the temperature higher than 70°C, the fan speed keeps in 100% PWM duty.
d. If set the hysteresis is 3°C (default 4°C), once the temperature becomes lower than 67°C, the fan speed would reduce to 90% PWM duty.

B. Stage auto mode (RPM%)

Set the temperature as 70°C, 60°C, 50°C, 40°C and the corresponding fan speed is 6,000 rpm, 5,400 rpm, 4,800 rpm, 4,200 rpm, and 3,600 rpm (assume the Max Fan Speed is 6,000 rpm).

Figure 13 Stage mode fan control illustration



a. Once the temperature is lower than 40°C, the lowest fan speed keeps in 3,600 rpm (60% of full speed).
b. Once the temperature is higher than 40°C, 50°C and 60°C, the fan speed will vary from 4,200 rpm to 5,400 rpm and increasing with the temperature level.
c. For the temperature higher than 70°C, the fan speed keeps in the full speed 6,000 rpm.
d. If the hysteresis is set as 3°C (default 4°C), once temperature gets lower than 67°C, the fan speed would reduce to 5,400 rpm.

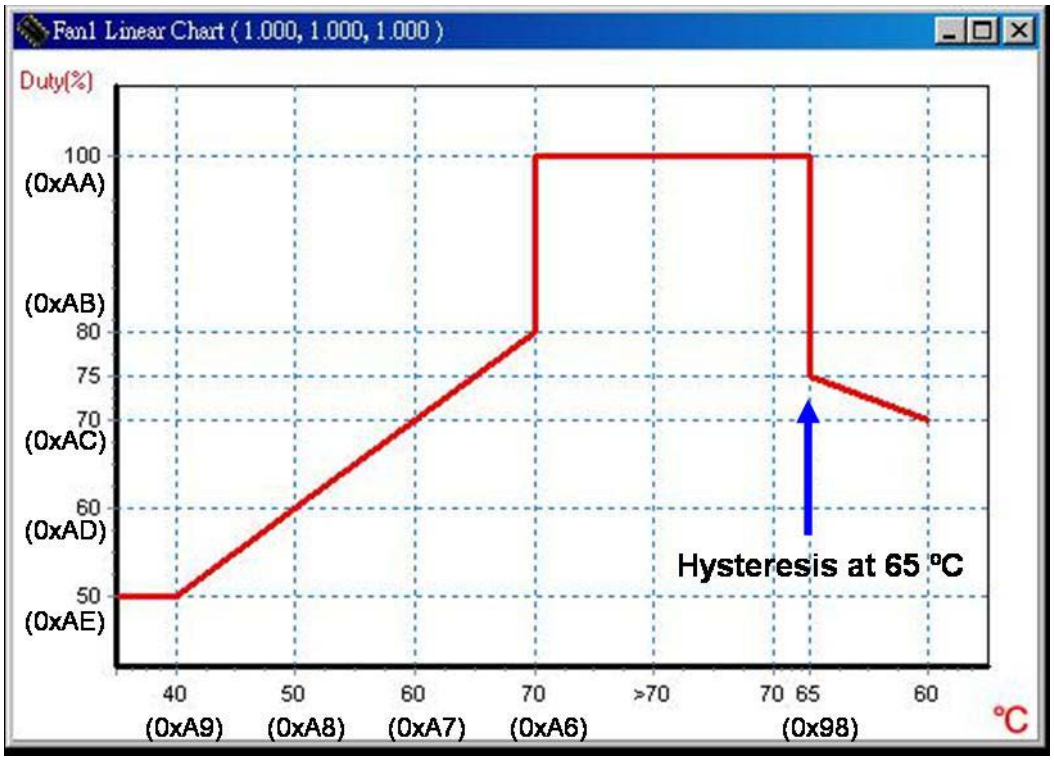
5.4.3.4 **Linear auto mode**

F81803 also supports linear auto mode. The fan speed would increase or decrease linearly with the temperature. There are also PWM Duty and RPM% modes for it.

A. Linear auto mode (PWM Duty)

Set the temperature as 70°C, 60°C, 50°C and 40°C and the duty is 100%, 80%, 70%, 60% and 50%.

Figure 14 Linear mode fan control illustration-1

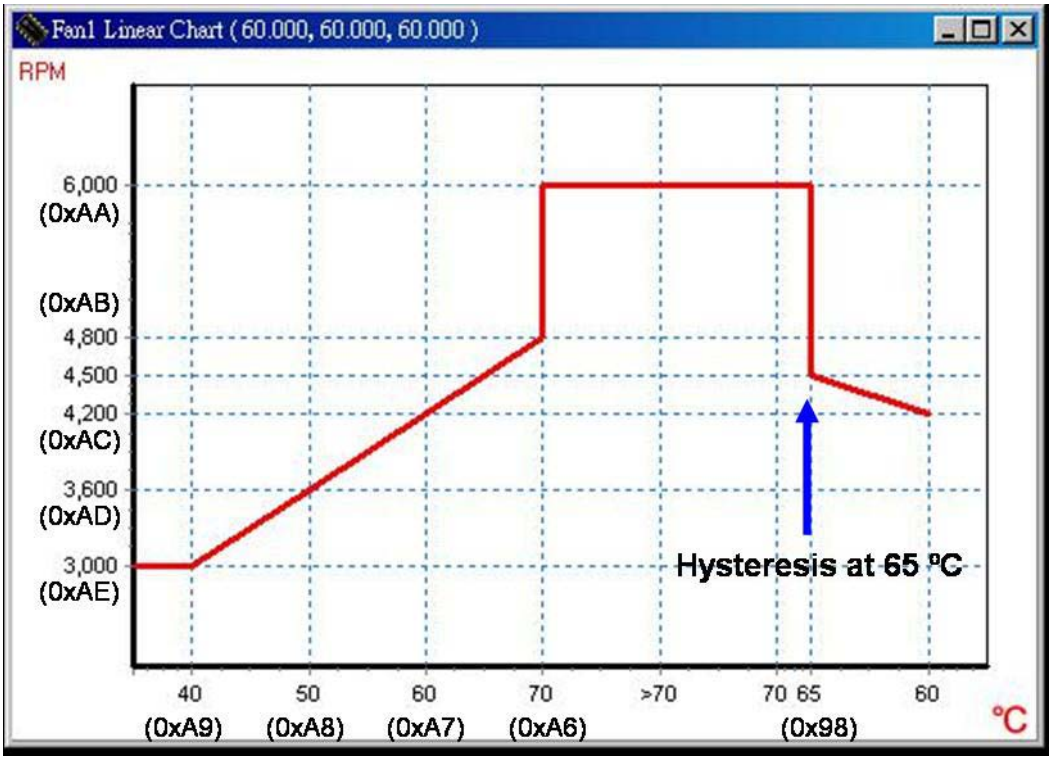


a. Once the temperature is lower than 40°C, the lowest fan speed keeps in the 50% PWM duty
b. Once the temperature becomes higher than 40°C, 50°C and 60°C, the fan speed will vary from 50% to 80% PWM duty linearly with the tempreature variation. The temp.-fan speed monitoring flash interval is 1sec.
c. Once the temperature goes over 70°C, the fan speed will directly increase to 100% PWM duty (full speed).
d. If set the hysteresis is 5°C (default is 4°C), once the temperature becomes lower than 65°C (instead of 70°C), the fan speed will reduce from 100% PWM duty and decrease linearly with the temperature.

B. Linear auto mode (RPM%)

Set the temperature as 70°C, 60°C, 50°C, 40°C and the corresponding fan speed is 6,000 rpm, 4,800 rpm, 4,200 rpm, 3,600 rpm and 3,000 rpm (assume the Max Fan Speed is 6,000 rpm).

Figure 15 Linear mode fan control illustration

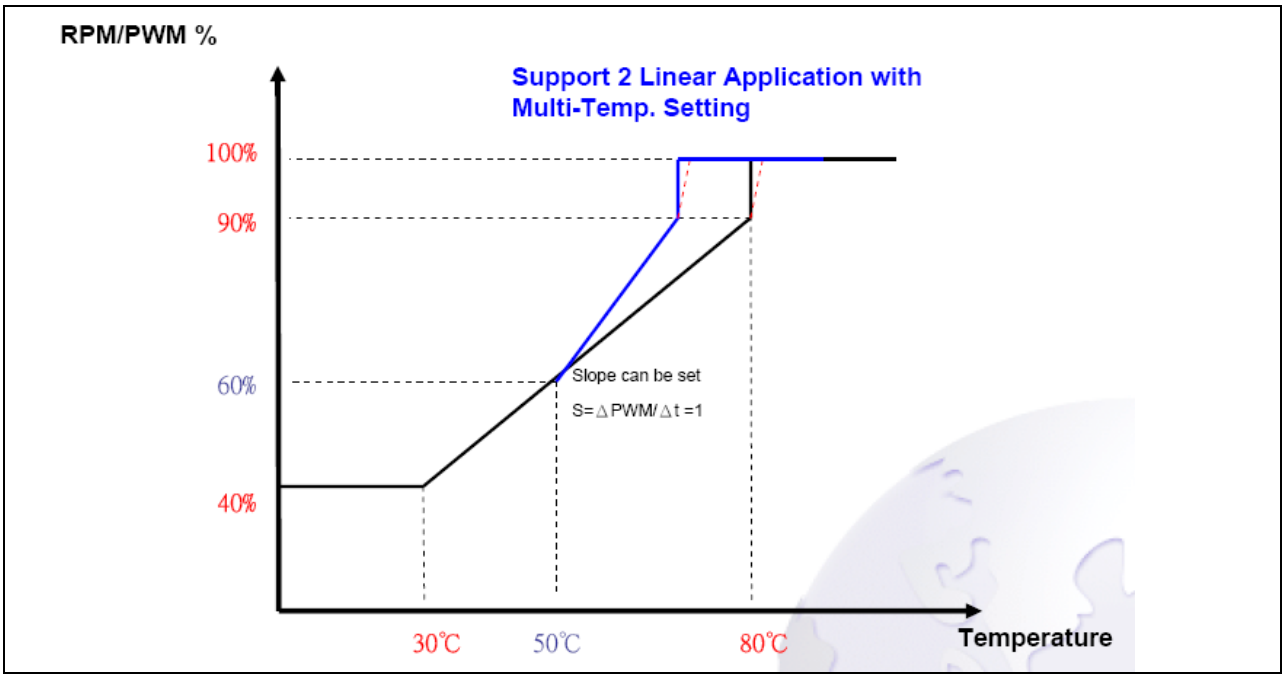


a. Once the temperature is lower than 40°C, the lowest fan speed keeps in 3,000 rpm (50% of full speed).
b. Once the temperature is over 40°C,50°C and 60°C, the fan speed will vary from 3,000 to 4,800 rpm almost linearly with the temperature variation because the temp.-fan speed monitoring flash interval is 1sec.
c. Once the temperature goes over 70°C, the fan speed will directly increase to full speed 6,000 rpm.
d. If the hysteresis is 5°C (default is 4°C), once the temperature becomes lower than 65°C (instead of 70°C), the fan speed wull reduce from full speed and decrease linearly with the temperature.

5.4.4 Fan Speed Control with Multi-temperature.

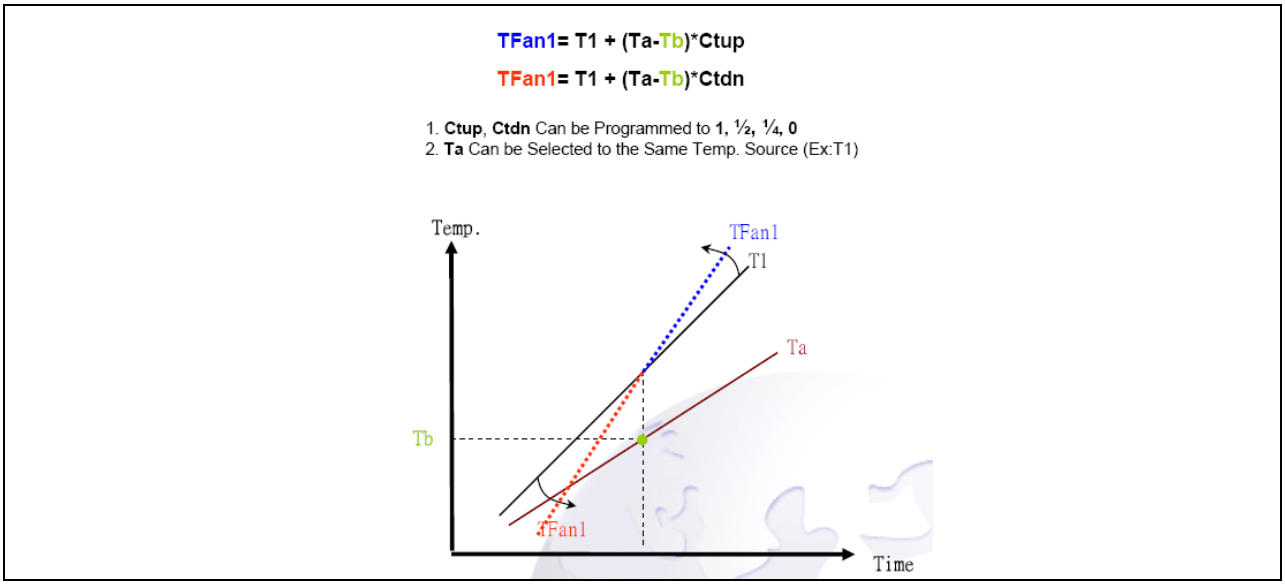
F81803 supports Multi-temperature for one fan control. This function works with linear auto mode can extend two linear slopes for one Fan control. As the graph below, this machine can support more silence fan control in low temperature environment and faster fan speed in high temperature segment. More detail setting please refers to the registers.

Figure 16 Multi-Temp Graph



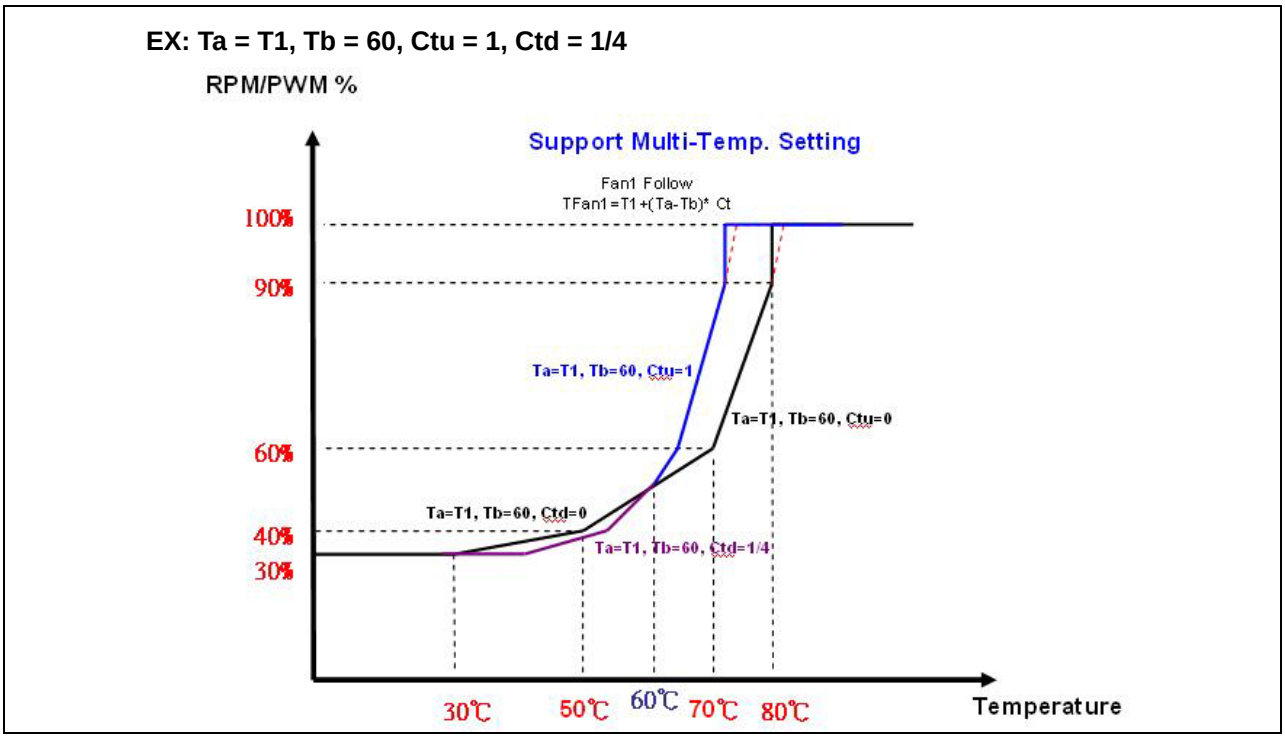
In the figure below, TFan1 is the scaled temperature for fan1. T1 is the real temperature for the fan1 sensor. Ta is another temperature data which can be used for linearly scale up or scale down the fan1 speed curve. Tb would be the point which starts the temperature scaling. The slope for the temperature curve over and under Tb would be Ctup and Ctdn.

Figure 17 Multi-Temp Graph



In application, we can set the Ta as the 2nd sensor temperature and Tb as the temperature which starts the scaling. So if the 2nd sensor temperature Ta is higher or lower than Tb, the fan1 speed would be changed with it.

Figure 18 Multi-Temp Graph

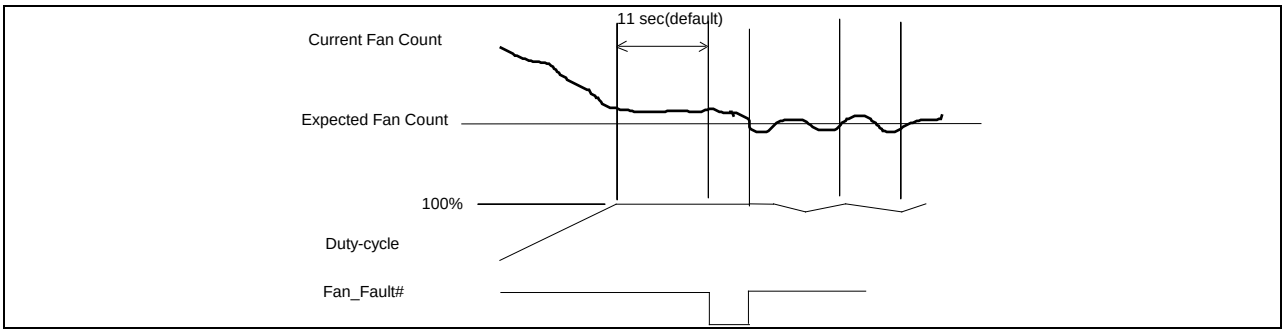


5.4.5 FAN_FAULT#

Fan_Fault# will be asserted when the fan speed doesn't meet the expected fan speed within a programmable period (default is 11 seconds) or when fan stops with respect to PWM duty-cycle which should be able to turn on the fan. There are two conditions may cause the FAN_FAULT# event.

(1). When PWM_Duty reaches 0xFF, the fan speed count can't reach the fan expected count in time.

Figure 19 FAN_FAULT# event



(2). After the period of detecting fan full speed, PWM_Duty > Min. Duty, fan count is still in 0xFFF.

5.1 ACPI

5.1.1 ACPI General Conception

The Advanced Configuration and Power Interface (ACPI) is a system for controlling the use of power in a computer. It lets computer manufacturer and user to determine the computer's power usage dynamically.

There are three ACPI states that are of primary concern to the system designer and they are designated S0, S3 and S5. S0 is a full-power state; the computer is being actively used in this state. The other two are called sleep states and reflect different power consumption when power-down. S3 is a state that the processor is powered down but the last procedural state is being stored in memory which is still active. S5 is a state that memory is off and the last procedural state of the processor has been stored to the hard disk. Take S3 and S5 as comparison, since memory is fast, the computer can quickly come back to full-power state, the disk is slower than the memory and the computer takes longer time to come back to full-power state. However, since the memory is off, S5 draws the minimal power comparing to S0 and S3.

ACPI includes three sub items as below:

1. Power Control Include:
   - PWOK Control Signal
   - Wake up via sleep state
   - Wake up stage detection
   - AC loss & resume control methods
2. EU Power Saving Function (EUP/ERP Command Lot 6.0)
2. Power Saving Mode

   Intel Power Saving Function (Deep Sleep Well, DSWl) and G3 Like Function

Where item 2 & 3 could be coexisted via ERP_CTRL# (follow SLP_SUS#), EUP/ERP mode could be achieved).

Before entering into the main section, let's check out the related hardware control signal first.

Control Signal	Power On/Off Control (AC Resume)	Power Management Event	Wake up	Intel DSW Hand Shaking	EUP/ERP Control
RSMRST#	◇				
S3#	◇				
S5#	◇				
PSIN#	◇				
PSOUT#	◇		☆★		
PS_ON#	◇				
PWOK	◇				

Control Signal	Power On/Off Control (AC Resume)	Power Management Event	Wake up	Intel DSW Hand Shaking	EUP/ERP Control
PME#		◇	☆★		
PS/2 KB/MS			☆★		
RI2#			☆★		
GPIO1x/4x			☆★		
SLP_SUS#				◇	
ERP_CTRL#				◇	◇

◇: Supported

★: Wake up via ERP

☆: Wake up via System

Power Control

5.1.1.1 Wake Up Stage Detection

F81803 is counted on the chipset SLP_S3#, SLP_S4#/SLP_S5# stage, to decide the wake up stage as below:

ACPI Stage	SLP_S3#	SLP_S4# /SLP_S5#
S0	H	H
S3	L	H
S5	L	L

H: High; L: Low

Power saving mode would be activated via CR0A index E0 bit 7.

5.1.1.2 Wake Up Via Sleep State

When the system is at the normal sleep state (S3, S4, S5) or deep sleep (G3') state, F81803 could wake up via PWSOUT# & PME#. See below for the related registers:

Wake up by PME#	Index 0x2D		CR0A Index 0xE0, 0xE8	CR0A Index 0xF0~0xF3
Normal Sleep State	◇			◇
EUP/ERP	◇		◇	
Wake up by PWSOUT#	Index 0x2D	CR 0A Index 0x30	CR0A Index 0xE0, 0xE8	CR0A Index 0xF4
Normal Sleep State	◇	◇		◇
EUP/ERP	◇	◇	◇	

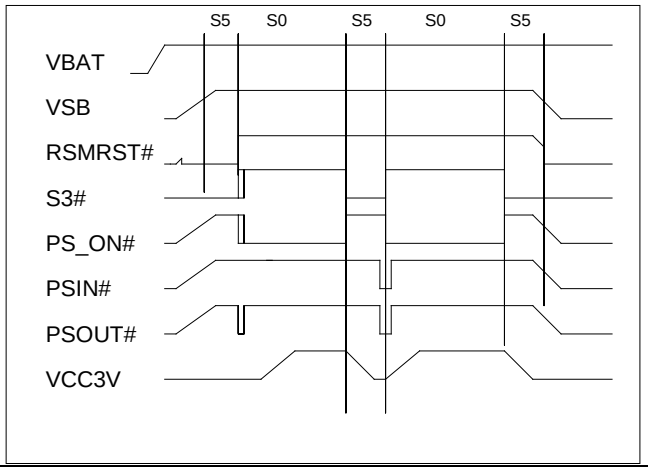
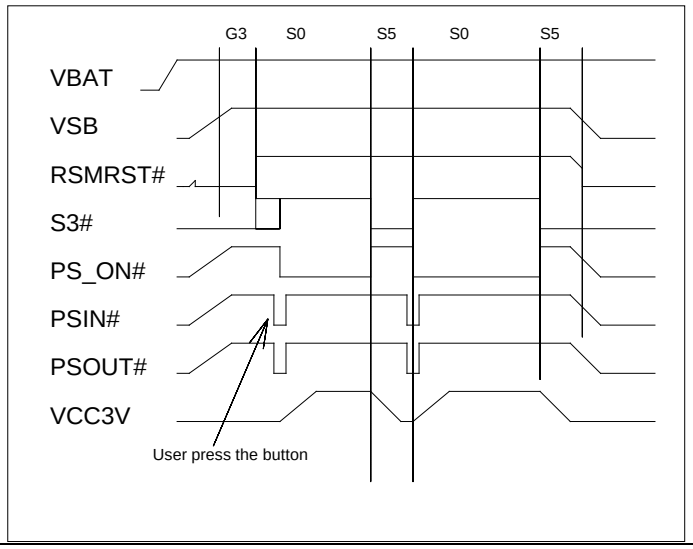
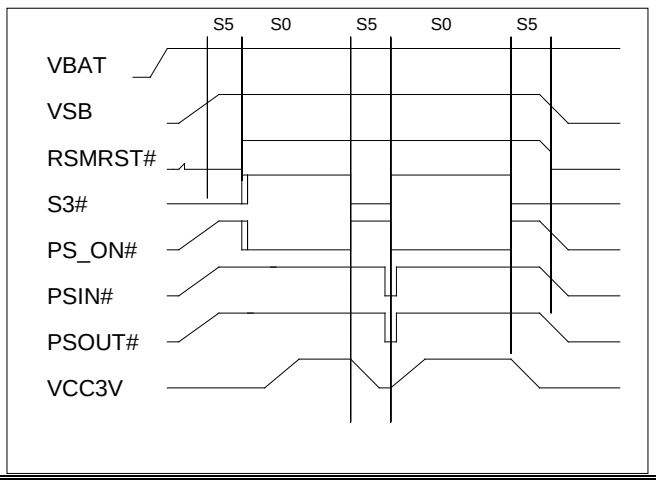
◇: Supported

5.1.1.3 AC Loss & Resume Control Methods

There are 5 modes under power loss state via setting ACPI control register, and they are Always On, Always Off, Bypass Mode, Keep Last State Mode 1 and Keep Last State Mode 2.

In Keep Last State Mode 1, one register will latch the status before power loss. If it is power on before power loss, it will automatically power on when power is resumed. If it is power off before power loss, it

will remain power off when power is resumed. See below for the detail:

Mode	Explanation
Always on (S0)	When AC resume, the system will power on automatically (send a PWSOUT# low pulse and then sinking the PS_ON# low). See below for the timing: 
Always off (S5)	When AC resume, the system is in off state and waiting for the wakeup events. See below for the timing: 
Bypass (follow the chipset after G3 stage)	When AC resume, inverting the S3 signal to PS_ON#. See below for the timing: 

<table>
<tr><th>Mode</th><th>Explanation</th></tr>
<tr><td>Keep Last State Mode</td><td>Using ATXPG_IN, VCC (PWOK), VSB (RSMRST) and S3 signals to detect the sleep state while AC loss occurs. One of the signal (ATXPG_IN, VCC or VSB under 2.8V) sinks low, SIO will latch the S3 signal to decide the system to be at “always on” or “always off” mode. See below table:
<table>
<tr><th>Signal
AC loss state</th><th>ATXPG</th><th>VCC</th><th>VSB</th><th>AC resume</th></tr>
<tr><td>AC loss in S0/S1 (S3=1)</td><td></td><td></td><td></td><td>Always on</td></tr>
<tr><td>AC loss in S3/S4/S5 (S3=0)</td><td></td><td></td><td></td><td>Always off</td></tr>
</table></td></tr>
<tr><td>Keep Last State Mode New Mode</td><td>Using VCC and S3 signals to detect the sleep state while AC loss occurs.
DPWOK signal sinks low after 1~2 second, SIO will latch the S3 signal to decide the system to be at “always on” or “always off” mode. See below table:
<table>
<tr><th>Signal
AC loss state</th><th>VCC</th><th>VSB</th><th>AC resume</th></tr>
<tr><td>AC loss in S0/S1 (S3=1)</td><td></td><td></td><td>Always on</td></tr>
<tr><td>AC loss in S3/S4/S5 (S3=0)</td><td></td><td></td><td>Always off</td></tr>
</table></td></tr>
</table>

5.1.2 Power Saving

In order to achieve the lower power consumption, the ERP_CTRL# could also turn off the 3VA so that the system can enter the Fintek G3’ state.

The F81803 supports Intel Chipset timing. There are 4 pins for CPT control: SUS_WARN#, SUS_ACK#, SLP_SUS# and DPWOK.

5.1.2.1 ErP Mode Select

ERP_CTRL# control the standby power rail on/off to fulfill the purpose which decreases the power consumption when the system in the sleep state or the soft-off state. Those two pins connected to the external PMOSs with default values are high in the sleep state in order to cut off all the standby power rails to save the power consumption. If the system needs to support wake-up function, those two pins can be programmable to set which power rail is turned on. The programmable register is powered by battery. So, the setting is kept even the AC power is lost when the register is set. At the power saving state (FINTEK calls it G3-like state), the F81803 consumes 5VSB power rail only to realize a low power consumption system.

Fintek provides 2 ErP modes, and they are Fintek G3’ mode, Intel DSW mode. The register for setting this mode is at CR0A, index 0xEC [7:6].

Bit	Name	Description
7-6	ERP_MODE	00: Fintek G3' mode. 01: Reserved. 10: Reserved. 11: Intel DSW mode.

5.1.3 Related Signals

5.1.3.1 PWOK Control Signal

PWOK are gated with VDD3VOK, ATXPG and S3#. PWOK is delayed 400ms (Default) when VCC arrives 2.8V, and the delay timing can be programmed by register. An additional programmable delay could be added to PWOK (0ms, 100ms, 200ms and 400ms).

Figure 20: F81803 Intel & AMD Mode PWOK Logic Sequence

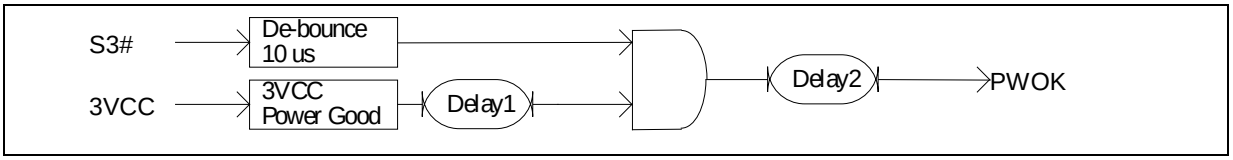


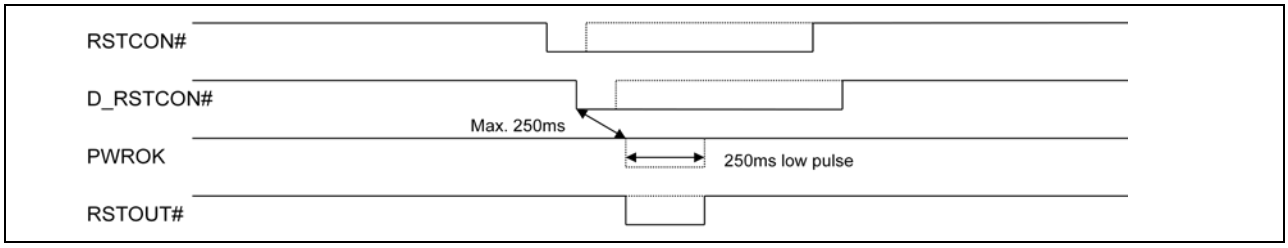
Table PWOK register setting guide

Delay	LDN 0x0A Index F5h	Description
Delay 1	VDD_DELAY	Bit [4-3]:The PWOK delay timing from 3VCCOK by followed setting 200ms (default)
Delay 2	PWOK_DELAY	Bit [7-6]: The additional PWOK delay. 200ms (default)

5.1.3.2 RSTCON# and RSTOUT# Function

F81803 has the RSTCON# / RSTOUT# function to reset the system. The function could be enabled in the register 0xF7 bit0 RSTOUT_EN. To enable this function, pin59 PCI_RST4# would change to the RSTOUT# and the pin61 RSTCON# would change to the RSTCON# function. Refer to the following Figure, we can choose whether PWOK or RSTOUT# would follow the RSTCON# low pulse and assert a 250 ms low pulse in register 0xF5 bit5. Also if the function is enabled, PCI_RST4# would not follow the LRESET# and PCI_RST5# would not follow the RSTCON# signal.

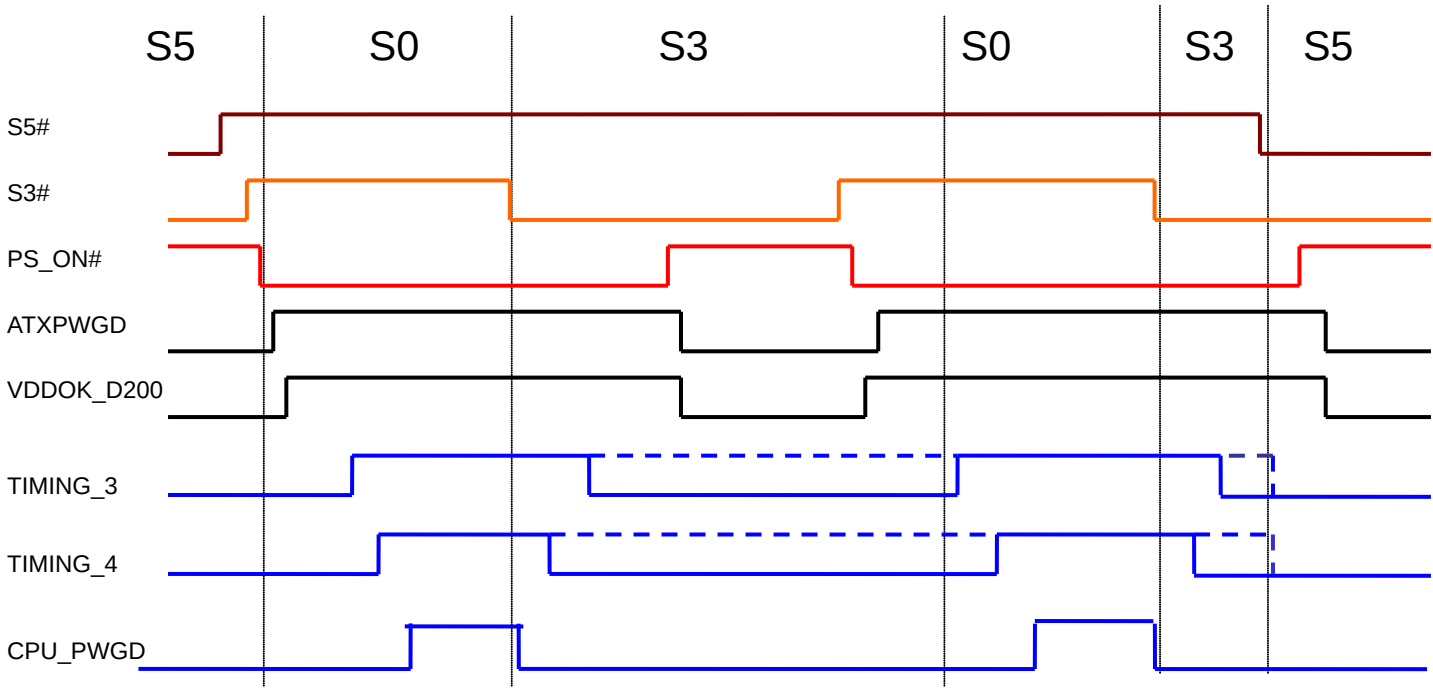
Figure 21: RSTCON and RSTOUR



5.2 AMD Power Timing Control Sequence

The F81803 offers 2 timing pins which are designed for AMD platform power sequence control including Vcore, and VLDT or other timing application purposes. All the timings on/off are relative to S3#/S5# and can be programmed by the register 0x0AF7. As shown in the below figure, the timings of TIMING_3~4 are displayed in blue lines.VDDOK_D400 is the PWOK delay timing from VDD3VOK. The default setting is that delay 400ms, there are 100ms, 200ms, and 300ms for option. It can be set in the register 0x0AF5.

Figure 22: Timing on/off sequence



5.3 Application Feature

5.3.1 PSIN# Detecting Flag

The purpose of PSIN# detecting flag is to detect the PSIN# exceeds the defined time or not. If exceeds the defined time, it could set a flag for BIOS usage. See below figures for detail:

Figure 23: Typical turn on Sequence

When the system is booting from S3/S4/S5 to S0, the typical sequence is send PSIN# pulse to PSOUT#. When the system is off from S0 to S3/S4/S5, 3VCC will be low after sends PSIN# pluse to PSOUT#.

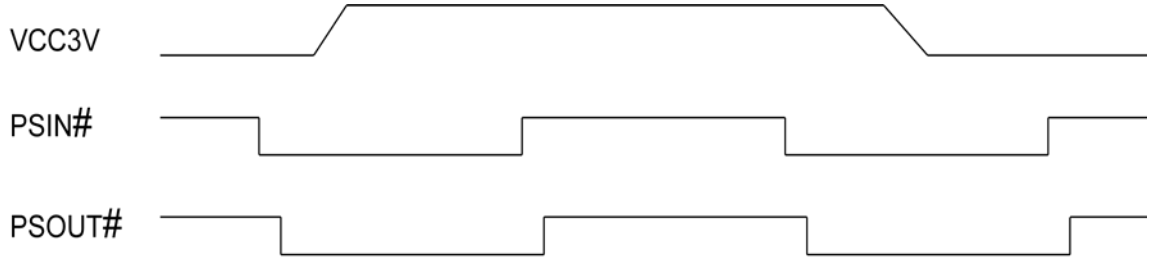


Figure 24: PSIN# Flag turn on detecting sequence

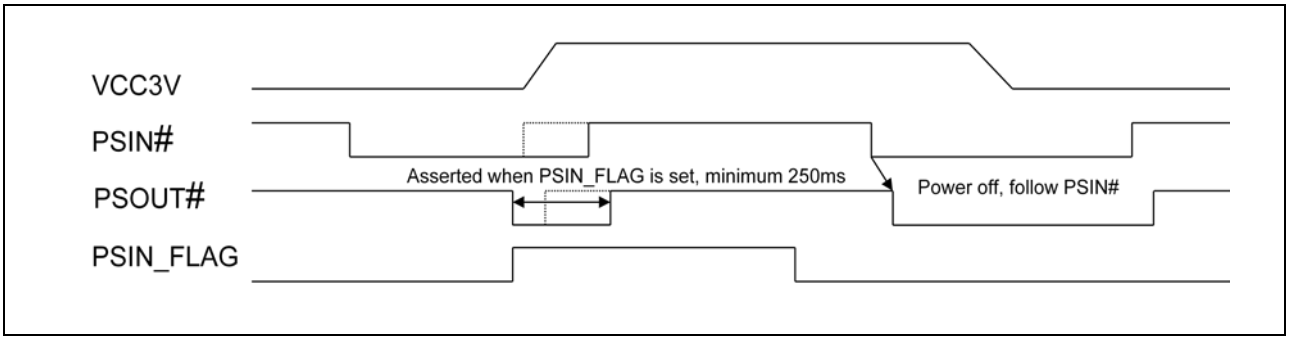
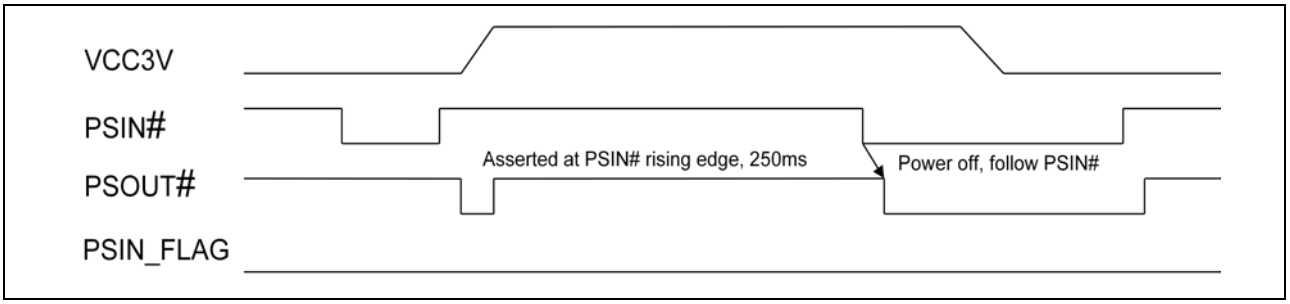


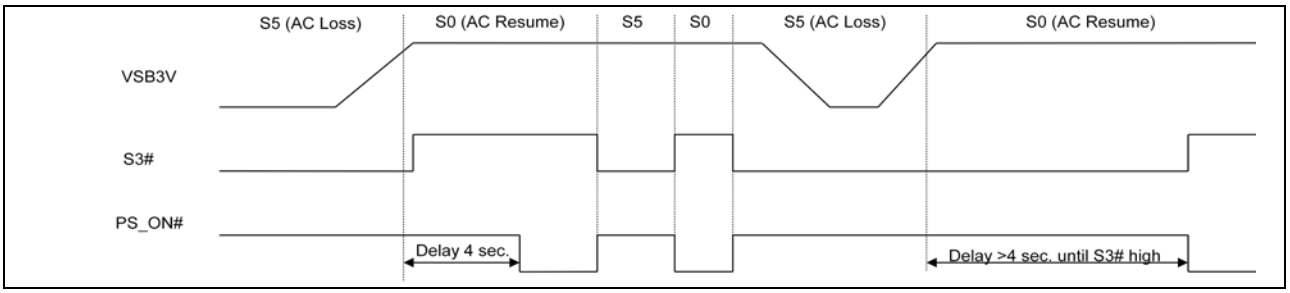
Figure 25: PSIN# Flag turn on detecting exceptional circumstance



5.3.2 Power-on Delay Function

The purpose of power-on delay 4 seconds function is protecting some PC cannot turn-on after AC resume. See the related register for the power on delay 4 seconds (Index 28[7]).

Figure 26: Delay Function



5.4 Keyboard Controller

The KBC circuit provides the functions included a keyboard and/or a PS/2 mouse, and can be used with IBM-compatible personal computers or PS/2-based systems. The controller receives serial data from the keyboard or PS/2 mouse, checks the parity of the data, and presents the data to the system as a byte of data in its output buffer. The controller will assert an interrupt to the system when data are placed in its output buffer.

5.4.1 Output Buffer

The output buffer is an 8-bit read-only register at I/O address 60h. The keyboard controller uses the output buffer to send the scan code received from the keyboard and data bytes required by commands to the system.

5.4.2 Input Buffer

The input buffer is an 8-bit write-only register at I/O address 60h or 64h. Writing to address 60h sets a flag to indicate a data write; writing to address 64h sets a flag to indicate a command write. Data written to I/O address 60h is sent to keyboard through the controller's input buffer only if the input buffer full bit in the status register is “0”.

5.4.3 Status Register

The status register is an 8-bit read-only register at I/O address 64h that holds information about the status of the keyboard controller and interface. It may be read at any time.

BIT	BIT FUNCTION	DESCRIPTION
0	Output Buffer Full	0: Output buffer empty 1: Output buffer full
1	Input Buffer Full	0: Input buffer empty 1: Input buffer full
2	System Flag	This bit may be set to 0 or 1 by writing to the system flag bit in the command byte of the keyboard controller (KCCB). It defaults to 0 after a power-on reset.
3	Command/Data	0: Data byte 1: Command byte
4	Inhibit Switch	0: Keyboard is inhibited 1: Keyboard is not inhibited
5	Mouse Output Buffer	0: Muse output buffer empty 1: Mouse output buffer full
6	General Purpose Time-out	0: No time-out error 1: Time-out error
7	Parity Error	0: Odd parity 1: Even parity (error)

5.4.4 Commands

<table>
<tr><th>COMMAND</th><th>FUNCTION</th></tr>
<tr><td>20h</td><td>Read Command Byte</td></tr>
<tr><td>60h</td><td>Write Command Byte
<table>
<tr><th>BIT</th><th>DESCRIPTION</th></tr>
<tr><td>0</td><td>Enable Keyboard Interrupt</td></tr>
<tr><td>1</td><td>Enable Mouse Interrupt</td></tr>
<tr><td>2</td><td>System flag</td></tr>
<tr><td>3</td><td>Reserve</td></tr>
<tr><td>4</td><td>Disable Keyboard Interface</td></tr>
<tr><td>5</td><td>Disable Mouse interface</td></tr>
<tr><td>6</td><td>IBM keyboard Translate Mode</td></tr>
<tr><td>7</td><td>Reserve</td></tr>
</table></td></tr>
<tr><td>A7h</td><td>Disable Auxiliary Device Interface</td></tr>
<tr><td>A8h</td><td>Enable Auxiliary Device Interface</td></tr>
<tr><td>A9h</td><td>Auxiliary Interface Test
8’h00: indicate Auxiliary interface is ok.
8’h01: indicate Auxiliary clock is low.
8’h02: indicate Auxiliary clock is high
8’h03: indicate Auxiliary data is low
8’h04: indicate Auxiliary data is high</td></tr>
<tr><td>AAh</td><td>Self-test
Return 55h if self test succeeds</td></tr>
<tr><td>ABh</td><td>keyboard Interface Test
8’h00: indicate keyboard interface is ok.
8’h01: indicate keyboard clock is low.
8’h02: indicate keyboard clock is high
8’h03: indicate keyboard data is low
8’h04: indicate keyboard data is high</td></tr>
<tr><td>ADh</td><td>Disable Keyboard Interface</td></tr>
<tr><td>AEh</td><td>Enable Keyboard Interface</td></tr>
<tr><td>C0h</td><td>Read Input Port(P1) and send data to the system</td></tr>
<tr><td>C1h</td><td>Continuously puts the lower four bits of Port1 into STATUS register</td></tr>
<tr><td>C2h</td><td>Continuously puts the upper four bits of Port1 into STATUS register</td></tr>
<tr><td>C8h</td><td>Enable Keyboard/Mouse swap.</td></tr>
<tr><td>C9h</td><td>Disable Keyboard/Mouse swap.</td></tr>
<tr><td>CAh</td><td>Read the data written by CBh command.</td></tr>
<tr><td>CBh</td><td>Written a scratch data. This byte could be read by CAh command.</td></tr>
<tr><td>D0h</td><td>Send Port2 value to the system</td></tr>
<tr><td>D1h</td><td>Only set/reset GateA20 line based on the system data bit 1</td></tr>
</table>

D2h	Send data back to the system as if it came from Keyboard
D3h	Send data back to the system as if it came from Muse
D4h	Output next received byte of data from system to Mouse
FEh	Low pulse on KBRST# about 6μS

KBC Command Description

5.4.5 PS/2 wakeup function

The KBC supports keyboard and mouse wakeup function. KBC will assert PME or PSOUT# signal. Those wakeup conditions are controlled by the configuration register.

5.5 GPIO

F81803 has 15 pins GPIO in total. All GPIO supports Input/Output control, Output data control, input status and Open Drain/Push Pull function selection. The GPIO05, GPIO06 and GPIO16 support interrupt status. The GPIO4x also support interrupt from SIRQ and wakeup event from PME# and PSOUT#. The GPIO2x supports the scan code function, please see registers for detail.

Scan Code Function

F81803 has 8 GPIO pins (GPIO 20~27) support scan code. These pins can not only set the volume up/down, mute and PWM up/down but also any function keys on keyboard. The protocol for these pins is scan code, so we don't need a driver to connect this function at OS. F81803 provides the programmable combination key as Clt+Alt+code for GPIO24~27.

5.5.1 GPIOx status

- Z means high impendence.
- If the external circuit is pull high then the pin status is "H"; else if the external circuit is pull low then the pin status is "L".
- "User define" means by programming the configuration register.

5.5.2 GPIO0x

Pin	Name	PIN Status				Register Power Well	Register Reset Signal	Pin Power Well
		G3 → S5	S0	S3	S5			
27	GPIO05	Z/User define	User define	User define	User define	VBAT	3VA/VBAT	3VA
28	GPIO06	Z/User define	User define	User define	User define	VBAT	3VA/VBAT	3VA

5.5.3 GPIO1x

Pin	Name	PIN Status				Register Power Well	Register Reset Signal	Pin Power Well
		G3 → S5	S0	S3	S5			

30	GPIO16	Z	User define	User define	User define	3VA	3VA	3VA

5.5.4 GPIO2x

Pin	Name	PIN Status				Register Power Well	Register Reset Signal	Pin Power Well
		G3 → S5	S0	S3	S5			
126	GPIO20	Z	User define	Z	Z	3VA	LRESET#	3VCC
127	GPIO21	Z	User define	Z	Z	3VA	LRESET#	3VCC
128	GPIO22	Z	User define	Z	Z	3VA	LRESET#	3VCC
1	GPIO23	Z	User define	Z	Z	3VA	LRESET#	3VCC
2	GPIO24	Z	User define	Z	Z	3VA	LRESET#	3VCC
3	GPIO25	Z	User define	Z	Z	3VA	LRESET#	3VCC
5	GPIO26	Z	User define	Z	Z	3VA	LRESET#	3VCC
6	GPIO27	Z	User define	Z	Z	3VA	LRESET#	3VCC

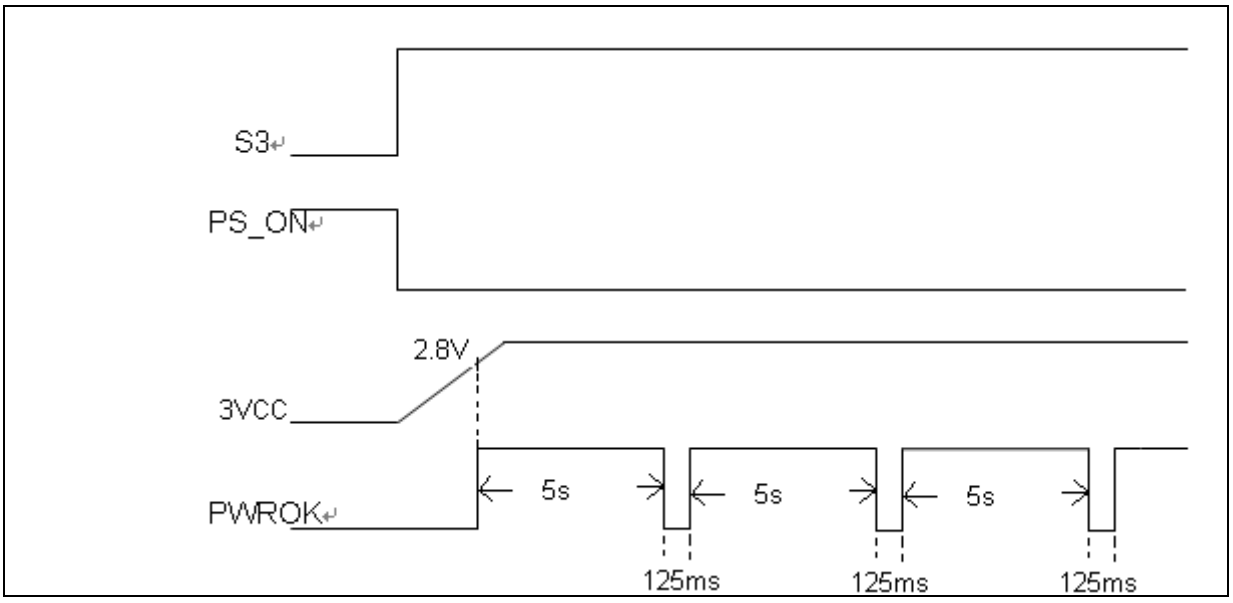
5.5.5 GPIO4x

Pin	Name	PIN Status				Register Power Well	Register Reset Signal	Pin Power Well
		G3 → S5	S0	S3	S5			
84	GPIO44	Z	User define	User define	User define	3VA	3VA	3VA
80	GPIO45	Z	User define	User define	User define	3VA	3VA	3VA
81	GPIO46	Z	User define	User define	User define	3VA	3VA	3VA
83	GPIO47	Z	User define	User define	User define	3VA	3VA	3VA

5.6 Watchdog Timer Function

Watch dog timer is provided for system controlling. If time-out can trigger one signal to high/low level/pulse, the signal is depend on register setting.

The time unit has two ways 1sec or 60sec. In pulse mode, there are four pulse widths can be selected (1ms/25ms/125ms/5sec). Please refer the device register description as below.



6 Register Description

The configuration register is used to control the behavior of the corresponding devices. To configure the register, using the index port to select the index and then writing data port to alter the parameters. The default index port and data port are 0x4E and 0x4F respectively. Pull down the SOUT1 pin to change the default value to 0x2E/0x2F. To enable configuration, the entry key 0x87 must be written to the index port. To disable configuration, write exit key 0xAA to the index port. Following is a example to enable configuration and disable configuration by using debug.

-o 4e 87

-o 4e 87 (enable configuration)

-o 4e aa (disable configuration)

The Following is a register map (total devices) grouped in hexadecimal address order, which shows a summary of all registers and their default value. Please refer each device chapter if you want more detail information.

Global Control Registers

"-" Reserved or Tri-State

Global Control Registers									
Register 0x[HEX]	**Register Name**	**Default Value**							
		MSB							**LSB**
02	Software Reset Register	-	-	-	-	-	-	-	-
07	Logic Device Number Register (LDN)	0	0	0	0	0	0	0	0
20	Chip ID Register 1	0	0	0	1	0	0	1	0
21	Chip ID Register 2	0	0	0	1	0	0	0	0
23	Vendor ID Register 1	0	0	0	1	1	0	0	1
24	Vendor ID Register 2	0	0	1	1	0	1	0	0
25	Software Power Down Register	-	-	-	-	-	0	0	-
26	Clock Select Register	0	-	0	-	0	0	0	0
27	Configuration Port Select Register	1	0	0	-	-	-	0	0
28	TSI Level Select Register (FUNC_PROG_SEL = 0)	1	1	1	-	0	-	-	-
29	TSI Pin Select Register (FUNC_PROG_SEL = 1)	0	0	0	0	0	0	0	0
29	Multi Function Select 1 Register	-	1	-	-	-	-	-	-
2A	Multi Function Select 2 Register	-	0	-	0	-	-	1	1
2B	Multi Function Select 3 Register	0	0	0	0	-	-	-	-
2C	Multi Function Select 4 Register	1	0	0	0	-	-	-	-
2D	Wakeup Control Register	-	-	-	0	1	0	0	0

Device Configuration Registers

"-" Reserved or Tri-State

UART1 Device Configuration Registers (LDN CR01)									
Register 0x[HEX]	**Register Name**	**Default Value**							
		MSB							**LSB**
30	UART1 Device Enable Register	-	-	-	-	-	-	-	1
60	Base Address High Register	0	0	0	0	0	0	1	1
61	Base Address Low Register	1	1	1	1	1	0	0	0

70	IRQ Channel Select Register	-	-	-	-	0	1	0	0
F0	IRQ Share Register	0	0	0	0	-	-	0	0
F2	Clock Source Select Register	-	-	-	-	-	-	0	0
F4	9-bit Mode Slave Address Register	0	0	0	0	0	0	0	0
F5	9-bit Mode Slave Address Mask Register	0	0	0	0	0	0	0	0
F6	FIFO Select Register	0	0	0	0	0	-	0	0
FF	9-bit Mode Broadcast Address Register	1	1	1	1	1	1	1	1

UART2 Device Configuration Registers (LDN CR02)

Register 0x[HEX]	Register Name	Default Value MSB							LSB
30	UART2 Device Enable Register	-	-	-	-	-	-	-	1
60	Base Address High Register	0	0	0	0	0	0	1	0
61	Base Address Low Register	1	1	1	1	1	0	0	0
70	IRQ Channel Select Register	-	-	-	-	0	1	0	0
F0	IRQ Share Register	0	0	0	0	-	-	0	0
F2	Clock Source Select Register	-	-	-	-	-	-	0	0
F4	9-bit Mode Slave Address Register	0	0	0	0	0	0	0	0
F5	9-bit Mode Slave Address Mask Register	0	0	0	0	0	0	0	0
F6	FIFO Select Register	0	0	0	0	0	-	0	0
FF	9-bit Mode Broadcast Address Register	1	1	1	1	1	1	1	1

Hardware Monitor Device Configuration Registers (LDN CR04)

Register 0x[HEX]	Register Name	Default Value MSB							LSB
30	H/W Monitor Device Enable Register	-	-	-	-	-	-	-	1
60	Base Address High Register	0	0	0	0	0	0	1	0
61	Base Address Low Register	1	0	0	1	0	1	0	1
70	IRQ Channel Select Register	-	-	-	-	0	0	0	0

KBC Device Configuration Registers (LDN CR05)

Register 0x[HEX]	Register Name	Default Value MSB							LSB
30	KBC Device Enable Register	-	-	-	-	-	-	-	1
60	Base Address High Register	0	0	0	0	0	0	0	0
61	Base Address Low Register	0	1	1	0	0	0	0	0
70	KB IRQ Channel Select Register	-	-	-	-	0	0	0	1
72	Mouse IRQ Channel Select Register	-	-	-	-	1	1	0	0
FE	PS/2 Swap Register	-	0	-	0	-	-	-	-

GPIO Device Configuration Registers (LDN CR06)

Register 0x[HEX]	Register Name	Default Value MSB							LSB
30	GPIO Device Enable Register	-	-	-	-	-	-	-	1
60	Base Address High Register	0	0	0	0	0	0	0	0
61	Base Address Low Register	0	0	0	0	0	0	0	0
70	GPIRQ Channel Select Register	-	-	-	-	0	0	0	0
F0	GPIO0 Output Enable Register	-	0	0	-	-	-	-	-

F1	GPIO0 Output Data Register	-	1	1	-	-	-	-	-
F2	GPIO0 Pin Status Register	-	-	-	-	-	-	-	-
F3	GPIO0 Drive Enable Register	-	0	0	-	-	-	-	-
F4	GPIO0 SMI Enable Register	-	0	0	-	-	-	-	-
F5	GPIO0 SMI Detect Select Register	-	1	1	-	-	-	-	-
F6	GPIO0 SMI Status Register	-	0	0	-	-	-	-	-
E0	GPIO1 Output Enable Register	-	0	-	-	-	-	-	-
E1	GPIO1 Output Data Register	-	1	-	-	-	-	-	-
E2	GPIO1 Pin Status Register	-	-	-	-	-	-	-	-
E3	GPIO1 Drive Enable Register	-	0	-	-	-	-	-	-
E4	GPIO1 SMI Enable Register	-	0	-	-	-	-	-	-
E5	GPIO1 SMI Detect Select Register	-	1	-	-	-	-	-	-
E6	GPIO1 SMI Status Register	-	0	-	-	-	-	-	-
D3	GPIO2 Drive Enable Register	0	0	0	0	0	0	0	0
B0	GPIO4 Output Enable Register	0	0	0	0	-	-	-	-
B1	GPIO4 Output Data Register	1	1	1	1	-	-	-	-
B2	GPIO4 Pin Status Register	-	-	-	-	-	-	-	-
B3	GPIO4 Drive Enable Register	0	0	0	0	-	-	-	-
B4	GPIO4 SMI Enable Register	-	-	-	-	0	0	0	0
B5	GPIO4 SMI Detect Select Register	-	-	-	-	0	0	0	0
B6	GPIO4 SMI Status Register	-	-	-	-	0	0	0	0
97	Scan Code Control Register 1	0	0	0	0	0	0	0	0
98	Scan Code Control Register 2	0	0	0	0	0	0	0	0
99	Scan Code Enable Register	1	1	1	1	1	1	1	1
9A	Break Code Enable Register	1	1	1	1	1	1	1	1
9B	Prefix Code Enable Register	1	1	1	1	1	1	1	1
9C	Make Code Register 0~7 (SCAN_BANK_SEL = 0~7)	0	0	0	0	0	0	0	0
9D	Prefix Code Register 0~7 (SCAN_BANK_SEL = 0~7)	1	1	1	0	0	0	0	0
9E	Make Code Status Register	0	0	0	0	0	0	0	0
9F	Break Code Status Register	0	0	0	0	0	0	0	0

WDT Device Configuration Registers (LDN CR07)

Register 0x[HEX]	Register Name	Default Value MSB							LSB
30	Watchdog device Base Address Enable Register	-	-	-	-	-	-	-	0
60	Base Address High Register	0	0	0	0	0	0	0	0
61	Base Address Low Register	0	0	0	0	0	0	0	0
F0	Watchdog Output Enable Register	0	-	-	-	-	-	-	-
F5	Watchdog Control Configuration Register 1	0	0	0	1	0	0	1	0
F6	Watchdog Timer Configuration Register 2	0	1	0	1	0	0	0	0
F7	Watchdog PME Enable Configuration Register 2	-	0	0	-	-	-	-	-

PME, ACPI, and ERP Power Saving Device Configuration Registers (LDN CR0A)

Register 0x[HEX]	Register Name	Default Value MSB							LSB
30	PME Device Enable Register	-	-	-	-	-	-	-	0

E0	ERP Enable Register	0	0	0	0	0	0	0	0
E1	ERP Control Register 1	-	-	-	0	-	1	-	0
E2	ERP Control Register 2	1	0	-	0	0	0	0	0
E3	ERP PSIN De-bounce Register	0	0	0	1	0	0	1	1
E4	ERP RSMRST De-bounce Register	0	0	0	0	1	0	0	1
E5	ERP PSOUT De-bounce Register	1	1	0	0	0	1	1	1
E6	ERP PS_ON De-bounce Register	0	0	0	0	1	0	0	1
E7	ERP Deep S5 Delay Register	0	1	1	0	0	0	1	1
E8	ERP Wakeup Enable Register	0	0	0	-	0	0	0	0
E9	ERP Deep S3 Delay Register	0	0	0	0	1	1	1	1
EC	ERP Mode Select Register	0	0	-	-	-	-	-	-
ED	ERP WDT Control Register	0	0	-	-	0	0	0	0
EE	ERP WDT Timer	0	0	0	0	0	0	0	0
F0	PME Event Enable 1 Register	0	0	0	0	-	0	0	-
F1	PME Event Status 1 Register	-	-	-	-	-	-	-	-
F2	PME Event Enable 2 Register	-	-	-	-	-	0	0	0
F3	PME Event Status 2 Register	-	-	-	-	-	-	-	-
F4	ACPI Control Register 1	0	0	0	0	0	1	1	1
F5	ACPI Control Register 2	1	0	-	0	1	-	0	0
F6	ACPI Control Register 3	0	0	0	-	-	-	-	-
F7	ACPI Control Register 4	-	-	0	0	0	-	-	-
F8	LED VCC Control Register	0	0	0	0	0	0	0	0
F9	LED VSB Control Register	0	0	0	0	0	0	0	0
FA	LED Additional Control Register	-	-	-	-	0	0	0	0
FB	ACPI Control Register 5	0	0	0	0	0	0	0	0
FC	ACPI Control Register 6	0	0	-	-	-	-	-	-
FE	RI De-bounce Select Register	-	-	-	-	-	-	0	0

6.1 Global Control Registers

6.1.1 Software Reset Register — Index 02h

Bit	Name	R/W	Reset	Default	Description
7-1	Reserved	-	-	-	Reserved
0	SOFT_RST	W	-	-	Write 1 to reset the register and device powered by VDD (3VCC).

6.1.2 Logic Device Number Register (LDN) — Index 07h

Bit	Name	R/W	Reset	Default	Description
7-0	LDN	R/W	LRESET#	00h	01h: Select UART1 device configuration registers. 02h: Select UART2 device configuration registers. 04h: Select Hardware Monitor device configuration registers. 05h: Select KBC device configuration registers. 06h: Select GPIO device configuration registers. 07h: Select WDT device configuration registers. 0Ah: Select PME, ACPI and ERP device configuration registers. Otherwise: Reserved.

6.1.3 Chip ID Register 1 — Index 20h

Bit	Name	R/W	Default	Description
7-0	Chip_ID1	R	12h	Chip ID1

6.1.4 Chip ID Register 2 — Index 21h

Bit	Name	R/W	Default	Description
7-0	Chip_ID2	R	10h	Chip ID2

6.1.5 Vendor ID Register 1 — Index 23h

Bit	Name	R/W	Default	Description
7-0	Vendor_ID1	R	19h	Vendor ID1

6.1.6 Vendor ID Register 2 — Index 24h

Bit	Name	R/W	Default	Description
7-0	Vendor_ID2	R	34h	Vendor ID2

6.1.7 Software Power Down Register — Index 25h

Bit	Name	R/W	Reset	Default	Description
7-3	Reserved	-	-	-	Reserved.
2	SOFTPD_UR2	R/W	3VCC	0	Write “1” to power down UART 2.
1	SOFTPD_UR1	R/W	3VCC	0	Write “1” to power down UART 1.
0	Reserved	-	-	-	Reserved.

6.1.8 Clock Select Register — Index 26h

Bit	Name	R/W	Reset	Default	Description
7	CLK_SEL	R/W	3VCC	0	The clock source of CLKIN. 0: CLKIN is 48MHz 1: CLKIN is 24MHz

6	Reserved	-	-	-	Reserved
5	DPORT_DEC_SEL	R/W	3VCC	0	Select the debug port address. 0: 0x80. 1: UART2 base address + 7. (UART 2 need to be enabled)
4	Reserved	-	-	-	Reserved
3	FUNC_PROG_SEL	R/W	3VCC	0	Index 0x29, 0x2B and 0x2C bank select register.
2-0	Reserved	R/W	3VCC	0	Dummy registers.

6.1.9 Configuration Port Select Register — Index 27h

Bit	Name	R/W	Reset	Default	Description
7	OVP_MODE	R/W	VBAT	1	OVP/UVP mode select. 0: OVP/UVP is auto enabled after power on. 1: OVP/UVP is enabled by registers.
6	TEMP_OUT_EN	R/W	LRESET#	0	Set this bit to “1” will output the CPU temperature to the 7-segment LED.
5	DPORT_EN	R/W	3VCC	0	0: The 80 port function is disabled. 1: The 80 port function is enabled.
4	PORT_4E_EN	R/W	3VCC	-	0: The configuration register port is 2E/2F. 1: The configuration register port is 4E/4F. This register is power on trapped by SOUT1/ STRAP4E_2E. Pull down to select port 2E/2F.
3-2	Reserved	-	-	-	Reserved
1	AT_ATX_MODE	R/W	VBAT	0	0: ATX mode. 1: AT mode. This register is power on trapped by AT_ATX_STRAP when 3VA power on.
0	TIMING_EN	R/W	VBAT	0	0: Disable power sequence. 1: Enable power sequence. This register is power on trapped by AT_ATX_STRAP when 3VA power on.

6.1.10 Configuration Port Select Register — Index 28h

Bit	Name	R/W	Reset	Default	Description
7	PWRON_4S_Delay	R/W	VBAT	0	0: Disable delay 4 sec function. 1: Enable delay 4 sec function When power on S3# delay 4 sec after AC resume.
6-0	Reserved	-	-	-	Reserved

6.1.11 TSI Level Select Register — Index 28h (FUNC_PROG_SEL = 0)

Bit	Name	R/W	Reset	Default	Description
7	S3_GATE_EN	R/W	VBAT	1	0: Pin 27 functions as GPIO05/WDTRST#. 1: Pin 27 functions as S3_GATE#.
6	GPIO06_EN	R/W	VBAT	1	0: Pin 28 functions as SCL. 1: Pin 28 functions as GPIO06.
5	GPIO05_EN	R/W	VBAT	1	This would be affected only if S3_GATE_EN is not set. 0: Pin 27 functions as WDTRST#. 1: Pin 27 functions as GPIO05.
4	Reserved	-	-	-	Reserved
3	TSI3_LVL_SEL	R/W	VBAT	0	Select MCLK/MDATA input level. 0: TTL level. 1: Low input level.
2-0	Reserved	-	-	-	Reserved

6.1.12 TSI Pin Select Register — Index 28h (FUNC_PROG_SEL = 1)

Bit	Name	R/W	Reset	Default	Description
7-6	Reserved	R/W	VBAT	0	Dummy registers.
5-4	TSI_PIN_SEL	R/W	VBAT	00	Select pins for TSI protocol. 00: Via pin 28 (GPIO06) /29 (PECI) if enabled. 11: Via pin 34 (MDATA) /35 (MCLK) if enabled. Others reserved.
3-2	MXM_PIN_SEL	R/W	VBAT	00	Select pins for MXM protocol. 00: Via pin 28 (GPIO06) /29 (PECI) if enabled. 11: Via pin 34 (MDATA) /35 (MCLK) if enabled. Others reserved.
1-0	I2C_PIN_SEL	R/W	VBAT	00	Select pins for I2C slave. 00: Via pin 28 (GPIO06) /29 (PECI) if enabled. 11: Via pin 34 (MDATA) /35 (MCLK) if enabled. Others reserved.

6.1.13 Multi Function Select 1 Register — Index 29h

Bit	Name	R/W	Reset	Default	Description
7	Reserved	-	-	-	Reserved
6	GPIO16_EN	R/W	VBAT	1	This bit only has effect if OVT_PIN_EN is not set. 0: Pin 30 functions as LED_VCC. 1: Pin 30 functions as GPIO16.
5-0	Reserved	-	-	-	Reserved

6.1.14 Multi Function Select 2 Register — Index 2Ah

Bit	Name	R/W	Reset	Default	Description
7	Reserved	-	-	-	Reserved
6	GP_WDT_RST_EN	R/W	VBAT	0	Set “1” to reset GPIO45_EN/GPIO46_EN when WDT timeout occurs.
5	Reserved	-	-	-	Reserved
4	OVT_PIN_EN	R/W	VBAT	0	0: Pin 30 functions as GPIO16/LED_VCC. 1: Pin 30 functions as OVT#.
3-2	Reserved	-	-	-	Reserved
1-0	UR2_GP_SEL	R/W	VBAT	11b	UART2 and GPIO2 multi-function select. This bit would be only effect if DPORT_EN is not set. When DPORT_EN is set, UART2 pins function as 7 segment LED control pins to display debug port value. 00: Full UART2. All pins are used for UART2. 01: Simple UART2. Only SIN2 and SOUT2 are used. 10: Modem control. RTS2#, RI2#, DSR2#, DCD2#, CTS2# and DTR2# are used. 11: Function as GPIO2.

6.1.15 Multi Function Select 3 Register — Index 2Bh

Bit	Name	R/W	Reset	Default	Description
7	GPIO47_EN	R/W	3VA	0	0: Pin 42 functions as PS_ON#. 1: Pin 42 functions as GPIO47.
6	GPIO46_EN	R/W	3VA	0	0: Pin 40 functions as PSOUT#. 1: Pin 40 functions as GPIO46. This bit could be reset by WDT timeout.
5	GPIO45_EN	R/W	3VA	0	0: Pin 39 functions as PSIN#. 1: Pin 39 functions as GPIO45. This bit could be reset by WDT timeout.
4	GPIO44_EN	R/W	3VA	0	0: Pin 43 functions as PWOK. 1: Pin 43 functions as GPIO44.
3-0	Reserved	-	-	-	Reserved

6.1.16 Multi Function Select 4 Register — Index 2Ch

Bit	Name	R/W	Reset	Default	Description
7	MS_PIN_EN	R/W	VBAT	1	0: Pin 34/35 function as SDA/SCL. 1: Pin 34/35 function as MDATA/MCLK.
6	GPIO0_RST_SEL	R/W	VBAT	0	0: GPIO0 registers are reset by 3VA. 1: GPIO0 registers are reset by VBAT.
5	SDA_PIN29_EN	R/W	VBAT	0	0: Pin 29 functions as PECI. 1: Pin 29 functions as SDA.
4	VCORE_RST_DIS	R/W	VBAT	0	0: VLDT_EN will force low when VCORE browns out. 1: VLDT_EN remain un-affected when VCORE browns out.

3-0	Reserved	-	-	-	Reserved

6.1.17 Wakeup Control Register — Index 2Dh

Bit	Name	R/W	Reset	Default	Description
7-5	Reserved	-	-	-	Reserved
4	KEY_SEL_ADD	R/W	VBAT	0	Refer to KEY_SEL.
3	WAKEUP_EN	R/W	VBAT	1	0: disable KB/Mouse wakeup function. 1: enable KB/Mouse wakeup function.
2-1	KEY_SEL	R/W	VBAT	00	Select the keyboard wakeup key. Accompany with KEY_SEL_ADD, there are several key select as below:
0	MO_SEL	R/W	VBAT	0	Select the mouse wakeup key. 0: Wakeup by clicking mouse. 1: Wakeup by mouse clicking or movement.

KEY_SEL_ADD	KEY_SEL	Wakeup Key
0	00	Ctrl + Esc
0	01	Ctrl + F1
0	10	Ctrl + Space
0	11	Any Key
1	00	Windows Wakeup Key
1	01	Windows Power Key
1	10	Ctrl + Alt + Space
1	11	Space

6.2 UART1 Registers (LDN 0x01)

6.2.1 Device Enable Register — Index 30h

Bit	Name	R/W	Reset	Default	Description
7-1	Reserved	-	-	-	Reserved
0	UR1_EN	R/W	LRESET#	1	0: disable UART 1 I/O Port. 1: enable UART 1 I/O Port.

6.2.2 Base Address High Register — Index 60h

Bit	Name	R/W	Reset	Default	Description
7-0	BASE_ADDR_HI	R/W	LRESET#	03h	The MSB of UART 1 base address.

6.2.3 Base Address Low Register — Index 61h

Bit	Name	R/W	Reset	Default	Description
7-0	BASE_ADDR_LO	R/W	LRESET#	F8h	The LSB of UART 1 base address.

6.2.4 IRQ Channel Select Register — Index 70h

Bit	Name	R/W	Reset	Default	Description
7-4	Reserved	-	-	-	Reserved.
3-0	SELUR1IRQ	R/W	LRESET#	4h	Select the IRQ channel for UART 1.

6.2.5 IRQ Share Register — Index F0h

Bit	Name	R/W	Reset	Default	Description
7	9BIT_MODE	R/W	LRESET#	0	0: normal UART function 1: enable 9-bit mode (multi-drop mode). In the 9-bit mode, the parity bit becomes the address/data bit.
6	AUTO_ADDR	R/W	LRESET#	0	This bit works only at 9-bit mode. 0: the SM2 bit will be cleared by host, so that data could be received. 1: the SM2 bit will be cleared by hardware according to the sent address and the given address (or broadcast address derived by SADDR and SADEN)
5	RS485_INV	R/W	LRESET#	0	Invert RTS# if RS485_EN is set.
4	RS485_EN	R/W	LRESET#	0	0: RS232 driver. 1: RS485 driver. RTS# is driven high automatically when transmitting data, otherwise it is keeping low.
3-2	Reserved	-	-	-	Reserved.
1	IRQ_MODE0	R/W	LRESET#	0	IRQ_MODE1 (UART1 FIFO Select Register — Index F6h, bit3) and IRQ_MODE0 will select the UART1 interrupt mode if IRQ sharing is enabled. 00 : Sharing IRQ active low Level mode. 01 : Sharing IRQ active high edge mode. 10 : Sharing IRQ active high Level mode. 11 : Reserved. This bit is effective at IRQ is sharing with the other device (IRQ_SHARE, bit 1).
0	IRQ_SHARE	R/W	LRESET#	0	0 : IRQ is not sharing with the other device. 1 : IRQ is sharing with the other device.

6.2.6 Clock Source Select Register — Index F2h

Bit	Name	R/W	Reset	Default	Description
7-2	Reserved	-	-	-	Reserved.
1-0	UR1_CLK_SEL	R/W	LRESET#	0	Select the clock source for UART1. 00: 1.8432MHz. 01: 18.432MHz. 10: 24MHz. 11: 14.769MHz.

6.2.7 9-bit Mode Slave Address Register — Index F4h

Bit	Name	R/W	Reset	Default	Description
7-0	SADDR	R/W	LRESET#	00h	This byte accompanying with SADEN will determine the given address and broadcast address at the 9-bit mode. The UART will response to both given and broadcast address. Following description determines the given address and broadcast address: 1. given address: If bit n of SADEN is “0”, then the corresponding bit of SADDR is don’t care. 2. broadcast address: If bit n of ORed SADDR and SADEN is “0”, don’t care that bit. The remaining bit which is “1” is compared to the received address. Broadcast address could be programmed by BADDR register, if BADDR is programmed broadcast address calculated by SADDR is ignored. Ex.

SADDR	0101_1100b
SADEN	1111_1001b
Given Address	0101_1xx0b
Broadcast Address	1111_11x1b

6.2.8 9-bit Mode Slave Address Mask Register — Index F5h

Bit	Name	R/W	Reset	Default	Description
7-0	SADEN	R/W	LRESET#	00h	This byte accompanying with SADDR will determine the given address and broadcast address in 9-bit mode. The UART will response to both given and broadcast address. Following description determines the given address and broadcast address: 3. given address: If bit n of SADEN is “0”, then the corresponding bit of SADDR is don’t care. 4. broadcast address: If bit n of ORed SADDR and SADEN is “0”, don’t care that bit. The remaining bit which is “1” is compared to the received address. Ex.

SADDR	0101_1100b
SADEN	1111_1001b
Given Address	0101_1xx0b
Broadcast Address	1111_11x1b

6.2.9 FIFO Select Register — Index F6h

Bit	Name	R/W	Reset	Default	Description
7	TX_DEL_1BIT	R/W	LREST#	0	0: TX will start transmit immediately after writing THR. 1: TX will delay 1 bit time to transmit after writing THR.
6	TX_INT_MODE	R/W	LRESET#	0	0: TX will assert interrupt when THR is empty. 1: TX will assert interrupt when THR and shift register is empty.
5-4	RXFTHR_MODE	R/W	LRESET#	0	The RX FIFO threshold select. 00: FIFO threshold is set by RXFTHR. 01: FIFO threshold will be 2X of RXFTHR. 10: FIFO threshold will be 4X of RXFTHR. 11: FIFO threshold will be 8X of RXFTHR.
3	IRQ_MODE1	R/W	LREST#	0	IRQ_MODE1 and IRQ_MODE0 (UART1 IRQ Share Register — Index F0h, bit1) will select the UART1 interrupt mode if IRQ sharing is enabled. 00 : Sharing IRQ active low Level mode. 01 : Sharing IRQ active high edge mode. 10 : Sharing IRQ active high Level mode. 11 : Reserved. This bit is effective at IRQ is sharing with the other device (IRQ_SHARE= 1, UART1 IRQ share register— index F0h, bit 0).
2	Reserved	-	-	-	Reserved.
1-0	FIFO_MODE	R/W	LRESET#	00h	Select the FIFO depth. 00: 16-byte FIFO. 01: 32-byte FIFO. 10: 64-byte FIFO. 11: 128-byte FIFO.

6.2.10 9-bit Mode Broadcast Address Register — Index FFh

Bit	Name	R/W	Reset	Default	Description
7-0	BADDR	R/W	LRESET#	FFh	Broadcast address for 9-bit mode. Write this byte to set broadcast address instead of the one calculated by SADDR.

6.3 UART2 Registers (LDN 0x02)

6.3.1 Device Enable Register — Index 30h

Bit	Name	R/W	Reset	Default	Description
7-1	Reserved	-	-	-	Reserved
0	UR2_EN	R/W	LRESET#	0	0: disable UART 2 I/O Port. 1: enable UART 2 I/O Port.

6.3.2 Base Address High Register — Index 60h

Bit	Name	R/W	Reset	Default	Description
7-0	BASE_ADDR_HI	R/W	LRESET#	02h	The MSB of UART 2 base address.

6.3.3 Base Address Low Register — Index 61h

Bit	Name	R/W	Reset	Default	Description
7-0	BASE_ADDR_LO	R/W	LRESET	F8h	The LSB of UART 2 base address.

6.3.4 IRQ Channel Select Register — Index 70h

Bit	Name	R/W	Reset	Default	Description
7-4	Reserved	-	-	-	Reserved.
3-0	SELUR2IRQ	R/W	LRESET#	3h	Select the IRQ channel for UART 2.

6.3.5 IRQ Share Register — Index F0h

Bit	Name	R/W	Reset	Default	Description
7-6	Reserved	-	-	-	Reserved.
5	RS485_INV	R/W	LRESET#	0	Invert RTS# if RS485_EN is set.
4	RS485_EN	R/W	LRESET#	0	0: RS232 driver. 1: RS485 driver. RTS# is driven high automatically when transmitting data, otherwise it's keeping low.
3	RXW4C_IR	R/W	LRESET#	0	0 : No reception delay when SIR is changed from TX to RX. 1 : Reception delay 4 character-time when SIR is changed from TX to RX.
2	TXW4C_IR	R/W	LRESET#	0	0 : No transmission delay when SIR is changed from RX to TX. 1 : Transmission delay 4 character-time when SIR is changed from RX to TX.
1	IRQ_MODE0	R/W	LRESET#	0	IRQ_MODE1 (UART2 FIFO Select Register — Index F6h, bit3) and IRQ_MODE0 will select the UART2 interrupt mode if IRQ sharing is enabled. 00 : Sharing IRQ active low Level mode. 01 : Sharing IRQ active high edge mode. 10 : Sharing IRQ active high Level mode. 11 : Reserved. This bit is effective at IRQ is sharing with the other device (IRQ_SHARE, bit 1).
0	IRQ_SHARE	R/W	LRESET#	0	0 : IRQ is not sharing with the other device. 1 : IRQ is sharing with the other device.

6.3.6 Clock Source Select Register — Index F2h

Bit	Name	R/W	Reset	Default	Description
7-2	Reserved	-	-	-	Reserved.
1-0	UR2_CLK_SEL	R/W	LRESET#	0	Select the clock source for UART2. 00: 1.8432MHz. 01: 18.432MHz. 10: 24MHz. 11: 14.769MHz.

6.3.7 9-bit Mode Slave Address Register — Index F4h

<table>
<tr><th>Bit</th><th>Name</th><th>R/W</th><th>Reset</th><th>Default</th><th>Description</th></tr>
<tr><td>7-0</td><td>SADDR</td><td>R/W</td><td>LRESET#</td><td>00h</td><td>This byte accompanying with SADEN will determine the given address and broadcast address in 9-bit mode. The UART will response to both given and broadcast address.
Following description determines the given address and broadcast address:
5. given address: If bit n of SADEN is “0”, then the corresponding bit of SADDR is don’t care.
6. broadcast address: If bit n of ORed SADDR and SADEN is “0”, don’t care that bit. The remaining bit which is “1” is compared to the received address. Broadcast address could be programmed by BADDR register, if BADDR is programmed, broadcast address calculated by SADDR is ignored.
Ex.
<table>
<tr><td>SADDR</td><td>0101_1100b</td></tr>
<tr><td>SADEN</td><td>1111_1001b</td></tr>
<tr><td>Given Address</td><td>0101_1xx0b</td></tr>
<tr><td>Broadcast Address</td><td>1111_11x1b</td></tr>
</table>
</td></tr>
</table>

6.3.8 9-bit Mode Slave Address Mask Register — Index F5h

<table>
<tr><th>Bit</th><th>Name</th><th>R/W</th><th>Reset</th><th>Default</th><th>Description</th></tr>
<tr><td>7-0</td><td>SADEN</td><td>R/W</td><td>LRESET#</td><td>00h</td><td>This byte accompanying with SADDR will determine the given address and broadcast address in 9-bit mode. The UART will response to both given and broadcast address.
Following description determines the given address and broadcast address:
7. given address: If bit n of SADEN is “0”, then the corresponding bit of SADDR is don’t care.
8. broadcast address: If bit n of ORed SADDR and SADEN is “0”, don’t care that bit. The remaining bit which is “1” is compared to the received address.
Ex.
<table>
<tr><td>SADDR</td><td>0101_1100b</td></tr>
<tr><td>SADEN</td><td>1111_1001b</td></tr>
<tr><td>Given Address</td><td>0101_1xx0b</td></tr>
<tr><td>Broadcast Address</td><td>1111_11x1b</td></tr>
</table>
</td></tr>
</table>

6.3.9 FIFO Select Register — Index F6h

Bit	Name	R/W	Reset	Default	Description
7	TX_DEL_1BIT	R/W	LREST#	0	0: TX will start transmit immediately after writing THR. 1: TX will delay 1 bit time to transmit after writing THR.
6	TX_INT_MODE	R/W	LRESET#	0	0: TX will assert interrupt when THR is empty. 1: TX will assert interrupt when THR and shift register is empty.

5-4	RXFTHR_MODE	R/W	LRESET#	0	The RX FIFO threshold select. 00: FIFO threshold is set by RXFTHR. 01: FIFO threshold will be 2X of RXFTHR. 10: FIFO threshold will be 4X of RXFTHR. 11: FIFO threshold will be 8X of RXFTHR.
3	IRQ_MODE1	R/W	LREST#	0	IRQ_MODE1 and IRQ_MODE0 (UART1 IRQ Share Register — Index F0h, bit1) will select the UART1 interrupt mode if IRQ sharing is enabled. 00 : Sharing IRQ active low Level mode. 01 : Sharing IRQ active high edge mode. 10 : Sharing IRQ active high Level mode. 11 : Reserved. This bit is effective at IRQ is sharing with the other device (IRQ_SHARE= 1, UART1 IRQ share register— index F0h, bit 0).
2	Reserved	-	-	-	Reserved.
1-0	FIFO_MODE	R/W	LRESET#	00h	Select the FIFO depth. 00: 16-byte FIFO. 01: 32-byte FIFO. 10: 64-byte FIFO. 11: 128-byte FIFO.

6.3.10 9-bit Mode Broadcast Address Register — Index FFh

Bit	Name	R/W	Reset	Default	Description
7-0	BADDR	R/W	LRESET#	FFh	Broadcast address for 9-bit mode. Write this byte to set broadcast address instead of the one calculated by SADDR.

6.4 UART Register

6.4.1 Receiver Buffer Register — Base + 0

Bit	Name	R/W	Reset	Default	Description
7-0	RBR	R	LRESET#	00h	The data received. Read only when LCR [7] is 0

6.4.2 Transmitter Holding Register — Base + 0

Bit	Name	R/W	Reset	Default	Description
7-0	THR	W	LRESET#	00h	Data to be transmitted. Write only when LCR [7] is 0

6.4.3 Divisor Latch (LSB) — Base + 0

Bit	Name	R/W	Reset	Default	Description
7-0	DLL	R/W	LRESET#	01h	Baud generator divisor low byte. Access only when LCR [7] is 1.

6.4.4 Divisor Latch (MSB) — Base + 1

Bit	Name	R/W	Reset	Default	Description
7-0	DLM	R/W	LRESET#	00h	Baud generator divisor high byte. Access only when LCR [7] is 1.

6.4.5 Interrupt Enable Register (IER) — Base + 1

Bit	Name	R/W	Reset	Default	Description
7-5	Reserved	-	-	-	Reserved.
4	SM2	R/WC	LRESET#	0	This bit is used only in 9-bit mode and always returns “0” when 9-bit mode is disabled. 0: The receiver could receive data byte. 1: The receiver could only receive address byte and issue an interrupt when the address is received.
3	EDSSI	R/W	LRESET#	0	Enable Modem Status Interrupt. Access only when LCR [7] is 0.
2	ELSI	R/W	LRESET#	0	Enable Line Status Error Interrupt. Access only when LCR [7] is 0.
1	ETBFI	R/W	LRESET#	0	Enable Transmitter Holding Register Empty Interrupt. Access only when LCR [7] is 0.
0	ERBFI	R/W	LRESET#	0	Enable Received Data Available Interrupt. Access only when LCR [7] is 0.

6.4.6 Interrupt Identification Register (IIR) — Base + 2

Bit	Name	R/W	Reset	Default	Description
7	FIFO_EN	R	LRESET#	0	0: FIFO is disabled 1: FIFO is enabled.
6	FIFO_EN	R	LRESET#	0	0: FIFO is disabled 1: FIFO is enabled.
5-4	Reserved	-	LRESET#	-	Reserved.
3-1	IRQ_ID	R	LRESET#	00	000: Interrupt is caused by Modem Status 001: Interrupt is caused by Transmitter Holding Register Empty 010: Interrupt is caused by Received Data Available. 110: Interrupt is caused by Character Timeout 011: Interrupt is caused by Line Status.
0	IRQ_PENDN	R	LRESET#	1	1: Interrupt is not pending. 0: Interrupt is pending.

6.4.7 FIFO Control Register — Base + 2

Bit	Name	R/W	Reset	Default	Description
7-6	RCV_TRIG	W	LRESET#	00	00: Receiver FIFO trigger level is 1. 01: Receiver FIFO trigger level is 4. 10: Receiver FIFO trigger level is 8. 11: Receiver FIFO trigger level is 14.
5-3	Reserved	-	LRESET#	-	Reserved.
2	CLRTX	R	LRESET#	0	Reset the transmitter FIFO.
1	CLRRX	R	LRESET#	0	Reset the receiver FIFO.

0	FIFO_EN	R	LRESET#	0	0: Disable FIFO. 1: Enable FIFO.

6.4.8 Line Control Register (LCR) — Base + 3

Bit	Name	R/W	Reset	Default	Description
7	DLAB	R/W	LRESET#	0	0: Divisor Latch can't be accessed. 1: Divisor Latch can be accessed via Base and Base+1.
6	SETBRK	R/W	LRESET#	0	0: Transmitter is in normal condition. 1: Transmit a break condition.
5	STKPAR	R/W	LRESET#	0	XX0: Parity Bit is disable 001: Parity Bit is odd. 011: Parity Bit is even 101: Parity Bit is logic 1 111: Parity Bit is logic 0
4	EPS	R/W	LRESET#	0	
3	PEN	R/W	LRESET#	0	
2	STB	R/W	LRESET#	0	0: Stop bit is one bit 1: When word length is 5 bit stop bit is 1.5 bit else stop bit is 2 bit
1-0	WLS	R/W	LRESET#	00	00: Word length is 5 bit 01: Word length is 6 bit 10: Word length is 7 bit 11: Word length is 8 bit

6.4.9 MODEM Control Register (MCR) — Base + 4

Bit	Name	R/W	Reset	Default	Description
7-5	Reserved	-	LRESET#	-	Reserved.
4	LOOP	R/W	LRESET#	0	0: UART in normal condition. 1: UART is internal loop back
3	OUT2	R/W	LRESET#	0	0: All interrupt is disabled. 1: Interrupt is enabled (disabled) by IER.
2	OUT1	R/W	LRESET#	0	Read from MSR[6] while in loop back mode
1	RTS	R/W	LRESET#	0	0: RTS# is forced to logic 1 1: RTS# is forced to logic 0
0	DTR	R/W	LRESET#	0	0: DTR# is forced to logic 1 1: DTR# is forced to logic 0

6.4.10 Line Status Register (LSR) — Base + 5

Bit	Name	R/W	Reset	Default	Description
7	RCR_ERR	R	LRESET#	0	0: No error in the FIFO when FIFO is enabled 1: Error in the FIFO when FIFO is enabled.
6	TEMT	R	LRESET#	1	0: Transmitter is in transmitting. 1: Transmitter is empty.
5	THRE	R	LRESET#	1	0: Transmitter Holding Register is not empty. 1: Transmitter Holding Register is empty.

4	BI	R	LRESET#	0	0: No break condition detected. 1: A break condition is detected.
3	FE	R	LRESET#	0	0: Data received has no frame error. 1: Data received has frame error.
2	PE	R	LRESET#	0	0: Data received has no parity error. 1: Data received has parity error.
1	OE	R	LRESET#	0	0: No overrun condition occurred. 1: An overrun condition occurred.
0	DR	R	LRESET#	0	0: No data is ready for read. 1: Data is received.

6.4.11 MODEM Status Register (MSR) — Base + 6

Bit	Name	R/W	Reset	Default	Description
7	DCD	R	-	-	Complement of DCD# input. In loop back mode, this bit is equivalent to OUT2 in MCR.
6	RI	R	-	-	Complement of RI# input. In loop back mode , this bit is equivalent to OUT1 in MCR
5	DSR	R	-	-	Complement of DSR# input. In loop back mode , this bit is equivalent to DTR in MCR
4	CTS	R	-	-	Complement of CTS# input. In loop back mode , this bit is equivalent to RTS in MCR
3	DDCD	R	LRESET#	0	0: No state changed at DCD#. 1: State changed at DCD#.
2	TERI	R	LRESET#	0	0: No Trailing edge at RI#. 1: A low to high transition at RI#.
1	DDSR	R	LRESET#	1	0: No state changed at DSR#. 1: State changed at DSR#.
0	DCTS	R	LRESET#	1	0: No state changed at CTS#. 1: State changed at CTS#.

6.4.12 Scratch Register — Base + 7

Bit	Name	R/W	Reset	Default	Description
7-0	SCR	R/W	LRESET#	00h	Scratch register.

6.5 Hardware Monitor Registers (LDN 0x04)

6.5.1 Hardware Monitor Configuration Registers — Index 30h

Bit	Name	R/W	Default	Description
7-1	Reserved	-	-	Reserved
0	HM_EN	R/W	1	0: disable Hardware Monitor. 1: enable Hardware Monitor.

6.5.2 Base Address High Register — Index 60h

Bit	Name	R/W	Default	Description
7-0	BASE_ADDR_HI	R/W	02h	The MSB of Hardware Monitor base address.

6.5.3 Base Address Low Register — Index 61h

Bit	Name	R/W	Default	Description
7-0	BASE_ADDR_LO	R/W	95h	The LSB of Hardware Monitor base address.

6.5.4 IRQ Channel Select Register — Index 70h

Bit	Name	R/W	Default	Description
7-4	Reserved	-	-	Reserved.
3-0	SELHMIRQ	R/W	0000	Select the IRQ channel for Hardware Monitor.

6.6 KBC Registers (LDN 0x05)

6.6.1 KBC Device Enable Register — Index 30h

Bit	Name	R/W	Reset	Default	Description
7-1	Reserved	-	-	-	Reserved
0	KBC_EN	R/W	3VCC	1	0: disable KBC. 1: enable KBC.

6.6.2 Base Address High Register — Index 60h

Bit	Name	R/W	Reset	Default	Description
7-0	BASE_ADDR_HI	R/W	LRESET#	00h	The MSB of KBC command port address. The address of data port is command port address + 4

6.6.3 Base Address Low Register — Index 61h

Bit	Name	R/W	Reset	Default	Description
7-0	BASE_ADDR_LO	R/W	LRESET#	60h	The LSB of KBC command port address. The address of data port is command port address + 4.

6.6.4 KB IRQ Channel Select Register — Index 70h

Bit	Name	R/W	Reset	Default	Description
7-4	Reserved	-	-	-	Reserved.
3-0	SELKIRQ	R/W	LRESET#	1h	Select the IRQ channel for keyboard interrupt.

6.6.5 Mouse IRQ Channel Select Register — Index 72h

Bit	Name	R/W	Reset	Default	Description
7-4	Reserved	-	-	-	Reserved.
3-0	SELMIRQ	R/W	LRESET#	Ch	Select the IRQ channel for PS/2 mouse interrupt.

6.6.6 PS/2 Swap Register — Index FEh

Bit	Name	R/W	Reset	Default	Description
7	Reserved	-	-	-	Reserved
6	RE_GEN_INT_EN	R/W	VBAT	0	Set “1” to auto re-generate interrupt every 500ms if interrupt is not serviced.
5	Reserved	-	-	-	Reserved, Fintek Internal Used Registers Only.
4	KB_MO_SWAP	R/W	VBAT	0	Keyboard Mouse Swap. 0: Keyboard/Mouse is not swapped. 1: Keyboard/Mouse is swapped. This bit could be programmed by user.
3-0	Reserved	-	-	-	Reserved, Fintek Internal Used Registers Only.

6.7 GPIO Registers (LDN 0x06)

6.7.1 GPIO IO Port Enable Register — Index 30h

Bit	Name	R/W	Reset	Default	Description
7-1	Reserved	-	-	-	Reserved
0	GPIO_EN	R/W	LRESET#	1	0: disable GPIO. 1: enable GPIO.

6.7.2 Base Address High Register — Index 60h

Bit	Name	R/W	Reset	Default	Description
7-0	BASE_ADDR_HI	R/W	LRESET#	0h	The MSB of GPIO base address.

6.7.3 Base Address Low Register — Index 61h

Bit	Name	R/W	Reset	Default	Description
7-0	BASE_ADDR_LO	R/W	LRESET#	0h	The LSB of GPIO base address.

6.7.4 IRQ Channel Select Register — Index 70h

Bit	Name	R/W	Reset	Default	Description
7-4	Reserved	-	-	-	Reserved.
3-0	SELGPIRQ	R/W	LRESET#	0h	Select the IRQ channel for GPIO.

6.7.5 GPIO0 Output Enable Register — Index F0h

Bit	Name	R/W	Reset	Default	Description
7	Reserved	-	-	-	Reserved
6	GPIO06_OE	R/W	3VA/ VBAT	0	0: GPIO06 is input. 1: GPIO06 is output.
5	GPIO05_OE	R/W	3VA/ VBAT	0	0: GPIO05 is input. 1: GPIO05 is output.
4-0	Reserved	-	-	-	Reserved

6.7.6 GPIO0 Output Data Register — Index F1h

Bit	Name	R/W	Reset	Default	Description
7	Reserved	-	-	-	Reserved
6	GPIO06_VAL	R/W	3VA/ VBAT	1	0: GPIO06 outputs 0 when in output mode. 1: GPIO06 outputs 1 when in output mode.
5	GPIO05_VAL	R/W	3VA/ VBAT	1	0: GPIO05 outputs 0 when in output mode. 1: GPIO05 outputs 1 when in output mode.
4-0	Reserved	-	-	-	Reserved

6.7.7 GPIO0 Pin Status Register — Index F2h

Bit	Name	R/W	**Reset**	Default	Description
7	Reserved	-	-	-	Reserved
6	GPIO06_IN	R	-	-	The pin status of GPIO06.
5	GPIO05_IN	R	-	-	The pin status of GPIO05.
4-0	Reserved	-	-	-	Reserved

6.7.8 GPIO0 Drive Enable Register — Index F3h

Bit	Name	R/W	Reset	Default	Description
7	Reserved	-	-	-	Reserved
6	GPIO06_DRV_EN	R/w	3VA/ VBAT	0	0: GPIO06 is open drain. 1: GPIO06 is push pull.
5	GPIO05_DRV_EN	R/w	3VA/ VBAT	0	0: GPIO05 is open drain. 1: GPIO05 is push pull.
4-0	Reserved	-	-	-	Reserved

6.7.9 GPIO0 SMI Enable Register — Index F4h

Bit	Name	R/W	Reset	Default	Description
7	Reserved	-	-	-	Reserved
6	GPIO06_SMI_EN	R/W	3VA/ VBAT	0	0: Disable SMI event. 1: Enable SMI event via PME# or SIRQ if GPIO06_SMI_ST is set.
5	GPIO05_SMI_EN	R/W	3VA/ VBAT	0	0: Disable SMI event. 1: Enable SMI event via PME# or SIRQ if GPIO05_SMI_ST is set.

4-0	Reserved	-	-	-	Reserved

6.7.10 GPIO0 SMI Detect Select Register — Index F5h

Bit	Name	R/W	Reset	Default	Description
7	Reserved	-	-	-	Reserved
6	GPIO06_DET_SEL	R/W	3VA/ VBAT	1	0: GPIO06 rising edge to set SMI status. 1: GPIO06 falling edge to set SMI status.
5	GPIO05_DET_SEL	R/W	3VA/ VBAT	1	0: GPIO05 rising edge to set SMI status. 1: GPIO05 falling edge to set SMI status.
4-0	Reserved	-	-	-	Reserved

6.7.11 GPIO0 SMI Status Register — Index F6h

Bit	Name	R/W	Reset	Default	Description
7	Reserved	-	-	-	Reserved
6	GPIO06_SMI_ST	R/WC	3VA	0	0: No SMI event. 1: A SMI event will set if GPIO06 input is changed. This bit is available in input mode. Write “1” to this bit will clear the status.
5	GPIO05_SMI_ST	R/WC	3VA	0	0: No SMI event. 1: A SMI event will set if GPIO05 input is changed. This bit is available in input mode. Write “1” to this bit will clear the status.
4-0	Reserved	-	-	-	Reserved

6.7.12 GPIO1 Output Enable Register — Index E0h

Bit	Name	R/W	Reset	Default	Description
7	Reserved	-	-	-	Reserved
6	GPIO16_OE	R/W	3VA	0	0: GPIO16 is in input mode. 1: GPIO16 is in output mode.
5-0	Reserved	-	-	-	Reserved

6.7.13 GPIO1 Output Data Register — Index E1h

Bit	Name	R/W	Reset	Default	Description
7	Reserved	-	-	-	Reserved
6	GPIO16_VAL	R/W	3VA	1	0: GPIO16 outputs 0 when in output mode. 1: GPIO16 outputs1 when in output mode.
5-0	Reserved	-	-	-	Reserved

6.7.14 GPIO1 Pin Status Register — Index E2h

Bit	Name	R/W	Reset	Default	Description
7	Reserved	-	-	-	Reserved
6	GPIO16_IN	R	-	-	The pin status of GPIO16.

5-0	Reserved	-	-	-	Reserved

6.7.15 GPIO1 Drive Enable Register — Index E3h

Bit	Name	R/W	Reset	Default	Description
7	Reserved	-	-	-	Reserved
6	GPIO16_DRV_EN	R/W	3VA	0	0: GPIO16 is open drain in output mode. 1: GPIO16 is push pull in output mode.
5-0	Reserved	-	-	-	Reserved

6.7.16 GPIO1 SMI Enable Register — Index E4h

Bit	Name	R/W	Reset	Default	Description
7	Reserved	-	-	-	Reserved
6	GPIO16_SMI_EN	R/W	3VA	0	0: Disable SMI event. 1: Enable SMI event via PME# or SIRQ if GPIO16_SMI_ST is set.
5-0	Reserved	-	-	-	Reserved

6.7.17 GPIO1 SMI Detect Select Register — Index E5h

Bit	Name	R/W	Reset	Default	Description
7	Reserved	-	-	-	Reserved
6	GPIO16_DET_SEL	R/W	3VA	1	0: GPIO16 rising edge to set SMI status. 1: GPIO16 falling edge to set SMI status.
5-0	Reserved	-	-	-	Reserved

6.7.18 GPIO1 SMI Status Register — Index E6h

Bit	Name	R/W	Reset	Default	Description
7	Reserved	-	-	-	Reserved
6	GPIO16_SMI_ST	R/WC	3VA	0	0: No SMI event. 1: A SMI event will set if GPIO16 input is changed. This bit is available in input mode. Write “1” to this bit will clear the status.
5-0	Reserved	-	-	-	Reserved

6.7.19 GPIO2 Output Enable Register — Index D0h

Bit	Name	R/W	Reset	Default	Description
7	GPIO27_OE	R/W	LRESET#	0	0: GPIO27 is in input mode. 1: GPIO27 is in output mode.
6	GPIO26_OE	R/W	LRESET#	0	0: GPIO26 is in input mode. 1: GPIO26 is in output mode.
5	GPIO25_OE	R/W	LRESET#	0	0: GPIO25 is in input mode. 1: GPIO25 is in output mode.
4-0	Reserved	-	-	-	Reserved.

6.7.20 GPIO2 Output Data Register — Index D1h

Bit	Name	R/W	Reset	Default	Description
7	GPIO27_VAL	R/W	LRESET#	1	0: GPIO27 outputs 0 when in output mode. 1: GPIO27 outputs1 when in output mode.
6	GPIO26_VAL	R/W	LRESET#	1	0: GPIO26 outputs 0 when in output mode. 1: GPIO26 outputs1 when in output mode.
5	GPIO25_VAL	R/W	LRESET#	1	0: GPIO25 outputs 0 when in output mode. 1: GPIO25 outputs 1 when in output mode.
4	GPIO24_VAL	R/W	LRESET#	1	0: GPIO24 outputs 0 when in output mode. 1: GPIO24 outputs 1 when in output mode.
3	GPIO23_VAL	R/W	LRESET#	1	0: GPIO23 outputs 0 when in output mode. 1: GPIO23 outputs 1 when in output mode.
2	GPIO22_VAL	R/W	LRESET#	1	0: GPIO22 outputs 0 when in output mode. 1: GPIO22 outputs 1 when in output mode.
1	GPIO21_VAL	R/W	LRESET#	1	0: GPIO21 outputs 0 when in output mode. 1: GPIO21 outputs 1 when in output mode.
0	GPIO20_VAL	R/W	LRESET#	1	0: GPIO20 outputs 0 when in output mode. 1: GPIO20 outputs 1 when in output mode.

6.7.21 GPIO2 Pin Status Register — Index D2h

Bit	Name	R/W	Reset	Default	Description
7	GPIO27_IN	R	-	-	The pin status of GPIO27.
6	GPIO26_IN	R	-	-	The pin status of GPIO26.
5	GPIO25_IN	R	-	-	The pin status of GPIO25.
4	GPIO24_IN	R	-	-	The pin status of GPIO24.
3	GPIO23_IN	R	-	-	The pin status of GPIO23.
2	GPIO22_IN	R	-	-	The pin status of GPIO22.
1	GPIO21_IN	R	-	-	The pin status of GPIO21.
0	GPIO20_IN	R	-	-	The pin status of GPIO20.

6.7.22 GPIO2 Drive Enable Register — Index D3h

Bit	Name	R/W	Reset	Default	Description
7	GPIO27_DRV_EN	R/W	LRESET#	0	0: GPIO27 is open drain in output mode. 1: GPIO27 is push pull in output mode.
6	GPIO26_DRV_EN	R/W	LRESET#	0	0: GPIO26 is open drain in output mode. 1: GPIO26 is push pull in output mode.
5	GPIO25_DRV_EN	R/W	LRESET#	0	0: GPIO25 is open drain in output mode. 1: GPIO25 is push pull in output mode.
4	GPIO24_DRV_EN	R/W	LRESET#	0	0: GPIO24 is open drain in output mode. 1: GPIO24 is push pull in output mode.
3	GPIO23_DRV_EN	R/W	LRESET#	0	0: GPIO23 is open drain in output mode. 1: GPIO23 is push pull in output mode.
2	GPIO22_DRV_EN	R/W	LRESET#	0	0: GPIO22 is open drain in output mode. 1: GPIO22 is push pull in output mode.

1	GPIO21_DRV_EN	R/W	LRESET#	0	0: GPIO21 is open drain in output mode. 1: GPIO21 is push pull in output mode.
0	GPIO20_DRV_EN	R/W	LRESET#	0	0: GPIO20 is open drain in output mode. 1: GPIO20 is push pull in output mode.

6.7.23 GPIO4 Output Enable Register — Index B0h

Bit	Name	R/W	Reset	Default	Description
7	GPIO47_OE	R/W	3VA	0	0: GPIO47 is input. 1: GPIO47 is output.
6	GPIO46_OE	R/W	3VA	0	0: GPIO46 is input. 1: GPIO46 is output.
5	GPIO45_OE	R/W	3VA	0	0: GPIO45 is input. 1: GPIO45 is output.
4	GPIO44_OE	R/W	3VA	0	0: GPIO44 is input. 1: GPIO44 is output.
3-0	Reserved	-	-	-	Reserved

6.7.24 GPIO4 Output Data Register — Index B1h

Bit	Name	R/W	Reset	Default	Description
7	GPIO47_VAL	R/W	3VA	1	0: GPIO47 outputs 0 when in output mode. 1: GPIO47 outputs 1 when in output mode.
6	GPIO46_VAL	R/W	3VA	1	0: GPIO46 outputs 0 when in output mode. 1: GPIO46 outputs 1 when in output mode.
5	GPIO45_VAL	R/W	3VA	1	0: GPIO45 outputs 0 when in output mode. 1: GPIO45 outputs 1 when in output mode.
4	GPIO44_VAL	R/W	3VA	1	0: GPIO44 outputs 0 when in output mode. 1: GPIO44 outputs 1 when in output mode.
3-0	Reserved	-	-	-	Reserved

6.7.25 GPIO4 Pin Status Register — Index B2h

Bit	Name	R/W	Reset	Default	Description
7	GPIO47_ST	R	-	-	The pin status of GPIO47.
6	GPIO46_ST	R	-	-	The pin status of GPIO46.
5	GPIO45_ST	R	-	-	The pin status of GPIO45.
4	GPIO44_ST	R	-	-	The pin status of GPIO44.
3-0	Reserved	-	-	-	Reserved

6.7.26 GPIO4 Drive Enable Register — Index B3h

Bit	Name	R/W	Reset	Default	Description
7	GPIO47_DRV_EN	R/W	3VA	0	0: GPIO47 is open drain. 1: GPIO47 is push pull.

6	GPIO46_DRV_EN	R/W	3VA	0	0: GPIO46 is open drain. 1: GPIO46 is push pull.
5	GPIO45_DRV_EN	R/w	3VA	0	0: GPIO45 is open drain. 1: GPIO45 is push pull.
4	GPIO44_DRV_EN	R/W	3VA	0	0: GPIO44 is open drain. 1: GPIO44 is push pull.
3-0	Reserved	-	-	-	Reserved

6.7.27 GPIO4 SMI Enable Register — Index B4h

Bit	Name	R/W	Reset	Default	Description
7-4	Reserved	-	-	-	Reserved
3	GPIO43_SMI_EN	R/W	LRESET#	0	0: Disable SMI event. 1: Enable SMI event via PME# or SIRQ if GPIO43_SMI_ST is set.
2	GPIO42_SMI_EN	R/W	LRESET#	0	0: Disable SMI event. 1: Enable SMI event via PME# or SIRQ if GPIO42_SMI_ST is set.
1	GPIO41_SMI_EN	R/W	LRESET#	0	0: Disable SMI event. 1: Enable SMI event via PME# or SIRQ if GPIO41_SMI_ST is set.
0	GPIO40_SMI_EN	R/W	LRESET#	0	0: Disable SMI event. 1: Enable SMI event via PME# or SIRQ if GPIO40_SMI_ST is set.

6.7.28 GPIO4 SMI Detect Select Register — Index B5h

Bit	Name	R/W	Reset	Default	Description
7-4	Reserved	-	-	-	Reserved
3	GPIO43_DET_SEL	R/W	LRESET#	1	0: GPIO43 rising edge to set SMI status. 1: GPIO43 falling edge to set SMI status.
2	GPIO42_DET_SEL	R/W	LRESET#	1	0: GPIO42 rising edge to set SMI status. 1: GPIO42 falling edge to set SMI status.
1	GPIO41_DET_SEL	R/W	LRESET#	1	0: GPIO41 rising edge to set SMI status. 1: GPIO41 falling edge to set SMI status.
0	GPIO40_DET_SEL	R/W	LRESET#	1	0: GPIO40 rising edge to set SMI status. 1: GPIO40 falling edge to set SMI status.

6.7.29 GPIO4 SMI Status Register — Index B6h

Bit	Name	R/W	Reset	Default	Description
7-4	Reserved	-	-	-	Reserved
3	GPIO43_SMI_ST	R/WC	LRESET#	0	0: No SMI event. 1: A SMI event will set if GPIO43 input is changed. This bit is available in input mode. Write “1” to this bit will clear the status.
2	GPIO42_SMI_ST	R/WC	LRESET#	0	0: No SMI event. 1: A SMI event will set if GPIO42 input is changed. This bit is available in input mode. Write “1” to this bit will clear the status.

1	GPIO41_SMI_ST	R/WC	LRESET#	0	0: No SMI event. 1: A SMI event will set if GPIO41 input is changed. This bit is available in input mode. Write “1” to this bit will clear the status.
0	GPIO40_SMI_ST	R/WC	LRESET#	0	0: No SMI event. 1: A SMI event will set if GPIO40 input is changed. This bit is available in input mode. Write “1” to this bit will clear the status.

6.7.30 Scan Code Control Register 1 — Index 97h

Bit	Name	R/W	Reset	Default	Description
7-6	REP_DEL_TIME	R/W	3VA	0	Delay time for repeating the make code. 00: 500 ~ 750ms. 01: 750 ~ 1000ms. 10: 1000 ~ 1250ms. 11: 1250 ~ 1500ms.
5-4	REP_TIME	R/W	3VA	0	Repeat time when the key is pressed. 00: 20 times per second. 01: 10 times per second. 10: 4 times per second. 11: 2 timers per second.
3	DIS_REP_EVENT	R/W	3VA	0	Disable repeating the make code when key is pressed.
2	Reserved	R/W	3VA	0	Dummy register.
1	PSEUDO_8048_EN	R/W	3VA	0	Set “1” to enable auto response to KBC command. It will return 0xFA, 0xAA for 0xFF command and 0xFA for other commands. This bit is used for GPIO scan code function without PS/2 keyboard.
0	GP_KB_EN	R/W	3VA	0	Set this bit to enable KeyBoard key emulation function.

6.7.31 Scan Code Control Register 2 — Index 98h

Bit	Name	R/W	Reset	Default	Description
7	CTRL_ALT_EN7	R/W	3VA	0	0: Make code/ break code are asserted when GPIO27 is pressed /released. 1: Ctrl + Alt are asserted before make/break code.
6	CTRL_ALT_EN6	R/W	3VA	0	0: Make code/ break code are asserted when GPIO26 is pressed /released. 1: Ctrl + Alt are asserted before make/break code.
5	CTRL_ALT_EN5	R/W	3VA	0	0: Make code/ break code are asserted when GPIO25 is pressed /released. 1: Ctrl + Alt are asserted before make/break code.
4	CTRL_ALT_EN4	R/W	3VA	0	0: Make code/ break code are asserted when GPIO24 is pressed /released. 1: Ctrl + Alt are asserted before make/break code.
3	Reserved	R/W	3VA	0	Reserved.
0	SCAN_BANK_SEL	R/W	3VA	0	Bank select to program pre-code and make code.

6.7.32 Scan Code Enable Register — Index 99h

Bit	Name	R/W	Reset	Default	Description
7	SCAN_EN7	R/W	3VA	1	Set “1” to enable GPIO27 scan code function.
6	SCAN_EN6	R/W	3VA	1	Set “1” to enable GPIO26 scan code function.
5	SCAN_EN5	R/W	3VA	1	Set “1” to enable GPIO25 scan code function.
4	SCAN_EN4	R/W	3VA	1	Set “1” to enable GPIO24 scan code function.
3	SCAN_EN3	R/W	3VA	1	Set “1” to enable GPIO23 scan code function.
2	SCAN_EN2	R/W	3VA	1	Set “1” to enable GPIO22 scan code function.
1	SCAN_EN1	R/W	3VA	1	Set “1” to enable GPIO21 scan code function.
0	SCAN_EN0	R/W	3VA	1	Set “1” to enable GPIO20 scan code function.

6.7.33 Break Code Enable Register — Index 9Ah

Bit	Name	R/W	Reset	Default	Description
7	BREAK_EN7	R/W	3VA	1	0: No break asserted when GPIO27 is released. (rising edge) 1. Break code is asserted when GPIO27 is released.
6	BREAK_EN6	R/W	3VA	1	0: No break asserted when GPIO26 is released. (rising edge) 1. Break code is asserted when GPIO26 is released.
5	BREAK_EN5	R/W	3VA	1	0: No break asserted when GPIO25 is released. (rising edge) 1. Break code is asserted when GPIO25 is released.
4	BREAK_EN4	R/W	3VA	1	0: No break asserted when GPIO24 is released. (rising edge) 1. Break code is asserted when GPIO24 is released.
3	BREAK_EN3	R/W	3VA	1	0: No break asserted when GPIO23 is released. (rising edge) 1. Break code is asserted when GPIO23 is released.
2	BREAK_EN2	R/W	3VA	1	0: No break asserted when GPIO22 is released. (rising edge) 1. Break code is asserted when GPIO22 is released.
1	BREAK_EN1	R/W	3VA	1	0: No break asserted when GPIO21 is released. (rising edge) 1. Break code is asserted when GPIO21 is released.
0	BREAK_EN0	R/W	3VA	1	0: No break asserted when GPIO20 is released. (rising edge) 1. Break code is asserted when GPIO20 is released.

6.7.34 Prefix Code Enable Register — Index 9Bh

Bit	Name	R/W	Reset	Default	Description
7	PRE_CODE_EN7	R/W	3VA	1	0: No prefix code before make/break code for GPIO27. 1. Prefix code is asserted before make/break code for GPIO27.
6	PRE_CODE_EN6	R/W	3VA	1	0: No prefix code before make/break code for GPIO26. 1. Prefix code is asserted before make/break code for GPIO26.
5	PRE_CODE_EN5	R/W	3VA	1	0: No prefix code before make/break code for GPIO25. 1. Prefix code is asserted before make/break code for GPIO25.
4	PRE_CODE_EN4	R/W	3VA	1	0: No prefix code before make/break code for GPIO24. 1. Prefix code is asserted before make/break code for GPIO24.
3	PRE_CODE_EN3	R/W	3VA	1	0: No prefix code before make/break code for GPIO23. 1. Prefix code is asserted before make/break code for GPIO23.
2	PRE_CODE_EN2	R/W	3VA	1	0: No prefix code before make/break code for GPIO22. 1. Prefix code is asserted before make/break code for GPIO22.

1	PRE_CODE_EN1	R/W	3VA	1	0: No prefix code before make/break code for GPIO21. 1. Prefix code is asserted before make/break code for GPIO21.
0	PRE_CODE_EN0	R/W	3VA	1	0: No prefix code before make/break code for GPIO20. 1. Prefix code is asserted before make/break code for GPIO20.

6.7.35 Make Code Register 0 — Index 9Ch (SCAN_BANK_SEL = 0)

Bit	Name	R/W	Reset	Default	Description
7-0	MAKE_CODE0	R/W	3VA	0	Make code for GPIO20. When GPIO20 is pressed (falling edge), this code is asserted via KBC. When GPIO20 is released (rising edge), this code + 0x80 (i.e. break code) is asserted via KBC.

6.7.36 Make Code Register 1 — Index 9Ch (SCAN_BANK_SEL = 1)

Bit	Name	R/W	Reset	Default	Description
7-0	MAKE_CODE1	R/W	3VA	0	Make code for GPIO21. When GPIO21 is pressed (falling edge), this code is asserted via KBC. When GPIO21 is released (rising edge), this code + 0x80 (i.e. break code) is asserted via KBC.

6.7.37 Make Code Register 2 — Index 9Ch (SCAN_BANK_SEL = 2)

Bit	Name	R/W	Reset	Default	Description
7-0	MAKE_CODE2	R/W	3VA	0	Make code for GPIO22. When GPIO22 is pressed (falling edge), this code is asserted via KBC. When GPIO22 is released (rising edge), this code + 0x80 (i.e. break code) is asserted via KBC.

6.7.38 Make Code Register 3 — Index 9Ch (SCAN_BANK_SEL = 3)

Bit	Name	R/W	Reset	Default	Description
7-0	MAKE_CODE3	R/W	3VA	0	Make code for GPIO23. When GPIO23 is pressed (falling edge), this code is asserted via KBC. When GPIO23 is released (rising edge), this code + 0x80 (i.e. break code) is asserted via KBC.

6.7.39 Make Code Register 4 — Index 9Ch (SCAN_BANK_SEL = 4)

Bit	Name	R/W	Reset	Default	Description
7-0	MAKE_CODE4	R/W	3VA	0	Make code for GPIO20. When GPIO24 is pressed (falling edge), this code is asserted via KBC. When GPIO24 is released (rising edge), this code + 0x80 (i.e. break code) is asserted via KBC.

6.7.40 Make Code Register 5 — Index 9Ch (SCAN_BANK_SEL = 5)

Bit	Name	R/W	Reset	Default	Description

7-0	MAKE_CODE5	R/W	3VA	0	Make code for GPIO25. When GPIO25 is pressed (falling edge), this code is asserted via KBC. When GPIO25 is released (rising edge), this code + 0x80 (i.e. break code) is asserted via KBC.

6.7.41 Make Code Register 6 — Index 9Ch (SCAN_BANK_SEL = 6)

Bit	Name	R/W	Reset	Default	Description
7-0	MAKE_CODE6	R/W	3VA	0	Make code for GPIO26. When GPIO26 is pressed (falling edge), this code is asserted via KBC. When GPIO26 is released (rising edge), this code + 0x80 (i.e. break code) is asserted via KBC.

6.7.42 Make Code Register 7 — Index 9Ch (SCAN_BANK_SEL = 7)

Bit	Name	R/W	Reset	Default	Description
7-0	MAKE_CODE7	R/W	3VA	0	Make code for GPIO27. When GPIO27 is pressed (falling edge), this code is asserted via KBC. When GPIO27 is released (rising edge), this code + 0x80 (i.e. break code) is asserted via KBC.

6.7.43 Prefix Code Register 0 — Index 9Dh (SCAN_BANK_SEL = 0)

Bit	Name	R/W	Reset	Default	Description
7-0	PRE_CODE0	R/W	3VA	E0h	Prefix code for GPIO20. This code is asserted before make/break code.

6.7.44 PRE Code Register 1 — Index 9Dh (SCAN_BANK_SEL = 1)

Bit	Name	R/W	Reset	Default	Description
7-0	PRE_CODE1	R/W	3VA	E0h	Prefix code for GPIO21. This code is asserted before make/break code.

6.7.45 PRE Code Register 2 — Index 9Dh (SCAN_BANK_SEL = 2)

Bit	Name	R/W	Reset	Default	Description
7-0	PRE_CODE2	R/W	3VA	E0h	Prefix code for GPIO22. This code is asserted before make/break code.

6.7.46 PRE Code Register 3 — Index 9Dh (SCAN_BANK_SEL = 3)

Bit	Name	R/W	Reset	Default	Description
7-0	PRE_CODE3	R/W	3VA	E0h	Prefix code for GPIO23. This code is asserted before make/break code.

6.7.47 PRE Code Register 4 — Index 9Dh (SCAN_BANK_SEL = 4)

Bit	Name	R/W	Reset	Default	Description
7-0	PRE_CODE4	R/W	3VA	E0h	Prefix code for GPIO24. This code is asserted before make/break code.

6.7.48 PRE Code Register 0 — Index 9Dh (SCAN_BANK_SEL = 5)

Bit	Name	R/W	Reset	Default	Description
7-0	PRE_CODE5	R/W	3VA	E0h	Prefix code for GPIO25. This code is asserted before make/break code.

6.7.49 PRE Code Register 6 — Index 9Dh (SCAN_BANK_SEL = 6)

Bit	Name	R/W	Reset	Default	Description
7-0	PRE_CODE6	R/W	3VA	E0h	Prefix code for GPIO26. This code is asserted before make/break code.

6.7.50 PRE Code Register 7 — Index 9Dh (SCAN_BANK_SEL = 7)

Bit	Name	R/W	Reset	Default	Description
7-0	PRE_CODE7	R/W	3VA	E0h	Prefix code for GPIO27. This code is asserted before make/break code.

6.7.51 Make Code Status Register — Index 9Eh

Bit	Name	R/W	Reset	Default	Description
7	SCAN7_MAKE_STS	R/W	LRESET#	0	The KeyBoard Key emulation status of make code by GPIO27. When KeyBoard Key emulation event occurs and the make code of this key is sent, this bit will be set to 1. SCAN7_MAKE_STS will be cleared after host reading IO port 0x0060. The status will continue to occur when the key is pressed. Delay time and repeat time are determined by REP_TIME and REP_DEL_TIME.
6	SCAN6_MAKE_STS	R/W	LRESET#	0	The KeyBoard Key emulation status of make code by GPIO26. When KeyBoard Key emulation event occurs and the make code of this key is sent, this bit will be set to 1. SCAN6_MAKE_STS will be cleared after host reading IO port 0x0060. The status will continue to occur when the key is pressed. Delay time and repeat time are determined by REP_TIME and REP_DEL_TIME.
5	SCAN5_MAKE_STS	R/W	LRESET#	0	The KeyBoard Key emulation status of make code by GPIO25. When KeyBoard Key emulation event occurs and the make code of this key is sent, this bit will be set to 1. SCAN5_MAKE_STS will be cleared after host reading IO port 0x0060. The status will continue to occur when the key is pressed. Delay time and repeat time are determined by REP_TIME and REP_DEL_TIME.
4	SCAN4_MAKE_STS	R/W	LRESET#	0	The KeyBoard Key emulation status of make code by GPIO24. When KeyBoard Key emulation event occurs and the make code of this key is sent, this bit will be set to 1. SCAN4_MAKE_STS will be cleared after host reading IO port 0x0060. The status will continue to occur when the key is pressed. Delay time and repeat time are determined by REP_TIME and REP_DEL_TIME.
3	SCAN3_MAKE_STS	R/W	LRESET#	0	The KeyBoard Key emulation status of make code by GPIO23. When KeyBoard Key emulation event occurs and the make code of this key is sent, this bit will be set to 1. SCAN3_MAKE_STS will be cleared after host reading IO port 0x0060. The status will continue to occur when the key is pressed. Delay time and repeat time are determined by REP_TIME and REP_DEL_TIME.

2	SCAN2_MAKE_STS	R/W	LRESET#	0	The KeyBoard Key emulation status of make code by GPIO22. When KeyBoard Key emulation event occurs and the make code of this key is sent, this bit will be set to 1. SCAN2_MAKE_STS will be cleared after host reading IO port 0x0060. The status will continue to occur when the key is pressed. Delay time and repeat time are determined by REP_TIME and REP_DEL_TIME.
1	SCAN1_MAKE_STS	R/W	LRESET#	0	The KeyBoard Key emulation status of make code by GPIO21. When KeyBoard Key emulation event occurs and the make code of this key is sent, this bit will be set to 1. SCAN1_MAKE_STS will be cleared after host reading IO port 0x0060. The status will continue to occur when the key is pressed. Delay time and repeat time are determined by REP_TIME and REP_DEL_TIME.
0	SCAN0_MAKE_STS	R/W	LRESET#	0	The KeyBoard Key emulation status of make code by GPIO20. When KeyBoard Key emulation event occurs and the make code of this key is sent, this bit will be set to 1. SCAN0_MAKE_STS will be cleared after host reading IO port 0x0060. The status will continue to occur when the key is pressed. Delay time and repeat time are determined by REP_TIME and REP_DEL_TIME.

6.7.52 Break Code Status Register — Index 9Fh

Bit	Name	R/W	Reset	Default	Description
7	SCAN7_BRK_STS	R/W	LRESET#	0	The KeyBoard Key emulation status of break code by GPIO27. When KeyBoard Key emulation event occurs and the break code of this key is sent, this bit will be set to 1. SCAN7_BRK_STS will be cleared after host reading IO port 0x0060.
6	SCAN6_BRK_STS	R/W	LRESET#	0	The KeyBoard Key emulation status of break code by GPIO26. When KeyBoard Key emulation event occurs and the break code of this key is sent, this bit will be set to 1. SCAN6_BRK_STS will be cleared after host reading IO port 0x0060.
5	SCAN5_BRK_STS	R/W	LRESET#	0	The KeyBoard Key emulation status of break code by GPIO25. When KeyBoard Key emulation event occurs and the break code of this key is sent, this bit will be set to 1. SCAN5_BRK_STS will be cleared after host reading IO port 0x0060.
4	SCAN4_BRK_STS	R/W	LRESET#	0	The KeyBoard Key emulation status of break code by GPIO24. When KeyBoard Key emulation event occurs and the break code of this key is sent, this bit will be set to 1. SCAN4_BRK_STS will be cleared after host reading IO port 0x0060.
3	SCAN3_BRK_STS	R/W	LRESET#	0	The KeyBoard Key emulation status of break code by GPIO23. When KeyBoard Key emulation event occurs and the break code of this key is sent, this bit will be set to 1. SCAN3_BRK_STS will be cleared after host reading IO port 0x0060.
2	SCAN2_BRK_STS	R/W	LRESET#	0	The KeyBoard Key emulation status of break code by GPIO22. When KeyBoard Key emulation event occurs and the break code of this key is sent, this bit will be set to 1. SCAN2_BRK_STS will be cleared after host reading IO port 0x0060.
1	SCAN1_BRK_STS	R/W	LRESET#	0	The KeyBoard Key emulation status of break code by GPIO21. When KeyBoard Key emulation event occurs and the break code of this key is sent, this bit will be set to 1. SCAN1_BRK_STS will be cleared after host reading IO port 0x0060.

0	SCAN0_BRK_STS	R/W	LRESET#	0	The KeyBoard Key emulation status of break code by GPIO20. When KeyBoard Key emulation event occurs and the break code of this key is sent, this bit will be set to 1. SCAN0_BRK_STS will be cleared after host reading IO port 0x0060.

6.8 Watch Dog Timer Registers (LDN 0x07)

6.8.1 WDT Device Base Address Enable Register — Index 30h

Bit	Name	R/W	Reset	Default	Description
7-1	Reserved	-	-	-	Reserved
0	WDT_EN	R/W	LRESET#	0	0: disable WDT base address. 1: enable WDT base address.

6.8.2 Base Address High Register — Index 60h

Bit	Name	R/W	Reset	Default	Description
7-0	BASE_ADDR_HI	R/W	LRESET#	00h	The MSB of WDT base address.

6.8.3 Base Address Low Register — Index 61h

Bit	Name	R/W	Reset	Default	Description
7-0	BASE_ADDR_LO	R/W	LRESET#	00h	The LSB of WDT base address.

6.8.4 Watchdog Output Enable Register — Index F0h

Bit	Name	R/W	Reset	Default	Description
7	WDOUT_EN	R/W	3VA	0	0: disable Watchdog time out output via WDTRST#. 1: enable Watchdog time out output via WDTRST#.
6-1	Reserved	-	-	-	Reserved

6.8.5 Watchdog Control Configuration Register 1 — Index F5h

Bit	Name	R/W	Reset	Default	Description
7	WD_CLK_SEL	R/W	3VA	0	0: Watchdog timer clock is 10Hz clock divided by CLKIN. 1: Watchdog timer clock is internal 10Hz clock.
6	WDTMOUT_STS	R/W	3VA	0	If watchdog timeout event occurred, this bit will be set to 1. Write a 1 to this bit will clear it to 0.
5	WD_EN	R/W	3VA	0	If this bit is set to 1, the counting of watchdog time is enabled.
4	WD_PULSE	R/W	3VA	1	Select output mode (0: level, 1: pulse) of WDTRST# by setting this bit.
3	WD_UNIT	R/W	3VA	0	Select time unit (0: 1sec, 1: 60 sec) of watchdog timer by setting this bit.
2	WD_HACTIVE	R/W	3VA	0	Select output polarity of WDTRST# (1: high active, 0: low active) by setting this bit.
1-0	WD_PSWIDTH	R/W	3VA	10b	Select output pulse width of WDTRST# 0: 1 ms 1: 30 ms 2: 150 ms 3: 6 sec

6.8.6 Watchdog Timer Configuration Register 2 — Index F6h

Bit	Name	R/W	Reset	Default	Description
7-0	WD_TIME	R/W	3VCC	5h	Time of watchdog timer (0~255)

6.8.7 Watchdog PME Enable Configuration Register 2 — Index F7h

Bit	Name	R/W	Reset	Default	Description
7	WDT_PME	R	3VA	-	The PME Status. This bit will set when WDT_PME_EN is set and the watchdog timer is 1 unit before time out (or time out).
6	WDT_PME_EN	R/W	3VA	0	0: Disable Watchdog PME. 1: enable Watchdog PME.
5	WDT_PME_ST	R/WC	3VA	0	When WDT_PME occurs, this bit will be set. Write “1” to clear.
4-0	Reserved	-	-	-	Reserved.

6.9 Watchdog Register

6.9.1 Watchdog PME Control Register — base address + 00h

Bit	Name	R/W	Reset	Default	Description
7	WDOUT_EN	R/W	3VA	1	0: disable Watchdog time out output via WDTRST#. 1: enable Watchdog time out output via WDTRST#.
6-0	Reserved	R/W	3VA	0	Reserved.

6.9.2 Watchdog Timer Configuration Register 1— base address + 05h

Bit	Name	R/W	Reset	Default	Description
7	WD_CLK_SEL	R/W	3VA	0	0: Watchdog timer clock is 10Hz clock divided by CLKIN. 1: Watchdog timer clock is internal 10Hz clock.
6	WDTMOUT_STS	R/W	3VA	0	If watchdog timeout event occurred, this bit will be set to 1. Write a 1 to this bit will clear it to 0.
5	WD_EN	R/W	3VA	0	If this bit is set to 1, the counting of watchdog time is enabled.
4	WD_PULSE	R/W	3VA	1	Select output mode (0: level, 1: pulse) of WDTRST# by setting this bit.
3	WD_UNIT	R/W	3VA	0	Select time unit (0: 1sec, 1: 60 sec) of watchdog timer by setting this bit.
2	WD_HACTIVE	R/W	3VA	0	Select output polarity of WDTRST# (1: high active, 0: low active) by setting this bit.
1-0	WD_PSWIDTH	R/W	3VA	10b	Select output pulse width of WDTRST# 0: 1 ms 1: 25 ms 2: 125 ms 3: 5 sec

6.9.3 Watchdog Timer Configuration Register 2 — base address + 06h

Bit	Name	R/W	Reset	Default	Description
7-0	WD_TIME	R/W	3VA	5h	Time of watchdog timer

6.9.4 Watchdog PME Control Register — base address + 07h

Bit	Name	R/W	Reset	Default	Description
7	WDT_PME	R	3VA	-	The PME Status. This bit will set when WDT_PME_EN is set and the watchdog timer is 1 unit before time out (or time out).
6	WDT_PME_EN	R/W	3VA	0	0: Disable Watchdog PME. 1: enable Watchdog PME.
5	WDT_PME_ST	R/WC	3VA	0	When WDT_PME occurs, this bit will be set. Write “1” to clear.
4-1	Reserved	-		-	Reserved.
0	CPU_CHG_STS	R/W	VBAT	0	This bit will be set at rising edge of pin 55. Write “1” to clear.

6.10 PME, ACPI, and ERP Power Saving Registers (LDN 0x0A)

6.10.1 PME Device Enable Register — Index 30h

Bit	Name	R/W	Reset	Default	Description
7-1	Reserved	-	-	-	Reserved
0	PME_EN	R/W	3VA	0	PME global enable register. 0: disable PME. 1: enable PME.

6.10.2 ERP Enable Register — Index E0h

Bit	Name	R/W	Reset	Default	Description
7	ERP_EN	R/W	VBAT	0	0: disable ERP function 1: enable ERP function
6	S3_BACK	R/W	VBAT	0	This bit will set “1” when system is back from S3 state.
5-2	Reserved	R/W	VBAT	0	Reserved
1	ERP_PME_EN	R/W	VBAT	0	PME event enable. 0: disable PME event. 1: enable PME event, when wakeup event is detected.
0	ERP_PSOUT_EN	R/W	VBAT	0	PSOUT# event enable. This bit has no function if ERP_PME_EN is set. 0: disable RING1 PSOUT# event. 1: enable RING1 PSOUT# event, when wakeup event is detected.

6.10.3 ERP Control Register 1 — Index E1h

Bit	Name	R/W	Reset	Default	Description
7-5	Reserved	-	-	-	Reserved for Fintek test mode.
4	S3 _ ERP_CTRL#_DIS	R/W	VBAT	0	If clear to “0” ERP_CTRL# will output Low when S3 state. Else If set to “1” ERP_CTRL# will output High when S3 state.
3	Reserved	-	-	-	Reserved
2	S5 _ ERP_CTRL#_DIS	R/W	VBAT	1	If clear to “0” ERP_CTRL# will output Low when S5 state. Else If set to “1” ERP_CTRL# will output High when S5 state.
1	Reserved	-	-	-	Reserved

0	AC_ ERP_CTRL#_DIS	R/W	VBAT	0	If clear to “0” ERP_CTRL# will output Low when after AC lost. Else If set to “1” ERP_CTRL# will output High when after AC lost.

6.10.4 ERP Control Register 2 — Index E2h

Bit	Name	R/W	Reset	Default	Description
7	AC_LOST	R/WC	3VA	1	This bit is AC lost status and writes 1 to this bit will clear it.
6	Reserved	R/W	VBAT	0	Dummy register
5	Reserved	-	-	-	Reserved
4	ERP_CTRL#_RSMRST_EN	R/W	VBAT	0	0: Disable ERP_CTRL# assert RSMRST low 1: Enable ERP_CTRL# assert RSMRST low
3-2	Reserved	R/W	VBAT	0	Dummy register.
1	RSMRST_DET_5V_DIS	R/W	VBAT	0	Device detects 5VA power ok (4.4V) and 3VSB become high, and after ~50ms de-bounce time RSMRST will become high. But when user set this bit to 1. RSMRST will not check 5VA power ok.
0	Reserved	R	VBAT	0	Dummy register.

6.10.5 ERP PSIN De-bounce Register — Index E3h

Bit	Name	R/W	Reset	Default	Description
7-0	PSIN_DEB_TIME	R/W	VBAT	13h	PSIN# de-bounce time & the unit is 1ms, default is 20ms.

6.10.6 ERP RSMRST De-bounce Register — Index E4h

Bit	Name	R/W	Reset	Default	Description
7-0	RSMRST_DEB_TIME	R/W	VBAT	9h	RSMRST internal de-bounce time. The unit is 1ms and default is 10ms.

6.10.7 ERP PSOUT Pulse Width Register — Index E5h

Bit	Name	R/W	Reset	Default	Description
7-0	PSOUT_PW	R/W	VBAT	C7h	PSOUT# output pulse width. The unit is 1ms and default is 200ms.

6.10.8 ERP PS_ON De-bounce Register — Index E6h (Powered by VBAT)

Bit	Name	R/W	Reset	Default	Description
7-0	PSON_DEB_TIME	R/W	VBAT	9h	PS_ON# de-bounce time. The unit is 1ms, default is 10ms.

6.10.9 ERP Deep S5 Delay Register — Index E7h

Bit	Name	R/W	Reset	Default	Description
7-0	DS5_DELAY_TIME	R/W	VBAT	63h	The delay time from S5 state to deep S5 state. The unit is 64ms and default is 6.4 sec. Deep S5 state will disable if this byte is “0”. Write “0h” to this byte will disable deep S5.

6.10.10 ERP Wakeup Enable Register — Index E8h

Bit	Name	R/W	Reset	Default	Description
7	RI2_WAKEUP_EN	R/W	VBAT	0	Enable RI2# PME# event to wakeup.
6	Reserved	R/W	VBAT	0	Dummy register.
5	RI1_WAKEUP_EN	R/W	VBAT	0	Enable RI1# PME# event to wakeup.
4	Reserved	-	-	-	Reserved.
3	GP_WAKEUP_EN	R/W	VBAT	0	Set this bit to enable GPIO event to wakeup system.
2	TMOUT_WAKEUP_EN	R/W	VBAT	0	Set this bit to enable Timeout event to wakeup system.
1	MO_WAKEUP_EN	R/W	VBAT	0	Set this bit to enable Mouse event to wakeup system.
0	KB_WAKEUP_EN	R/W	VBAT	0	Set this bit to enable Keyboard event to wakeup system.

6.10.11 ERP Deep S3 Delay Register — Index E9h

Bit	Name	R/W	Reset	Default	Description
7-0	DS3_DELAY_TIME	R/W	VBAT	Fh	The delay time from S3 state to deep S3 state. The unit is 64ms and default is 1.024 sec. Deep S3 state will disable if this byte is “0”. Write “0h” to this byte will disable deep S3.

6.10.12 ERP Mode Select Register — Index ECh

Bit	Name	R/W	Reset	Default	Description
7-6	ERP_MODE	R/W	VBAT	0	00: Fintek G3’ mode. 01: Reserved. 10: Reserved. 11: Intel DSW mode.
5-0	Revered	-	-	-	Reserved.

6.10.13 ERP WDT Control Register — Index EDh

Bit	Name	R/W	Reset	Default	Description
7-6	WDT_TIME[11:10]	R/W	VBAT	0	Bit 11 and 10 of WDT_TIME
5	Revered	-	-	-	Reserved.
4	WD_TMOUT	R/W	VBAT	-	ERP watchdog timer timeout status. Write 1 to clear.
3-2	WDT_TIME[9:8]	R/W	VBAT	0	Bit 9 and 8 of WDT_TIME
1	WD_UNIT	R/W	VBAT	0	0: unit of WD_TIME is 1 sec. 1: unit of WD_TIME is 1 minute.
0	WD_EN	R/W	VBAT	0	Enable ERP watchdog timer.

6.10.14 ERP WDT Time Register — Index EEh

Bit	Name	R/W	Reset	Default	Description
7-0	WD_TIME[7:0]	R/W	VBAT	0	ERP watchdog timer count time register. Start to count down when WD_EN is set. When reaching 0, WD_EN will auto clear and WD_TMOUT is set. A wakeup event will assert if enabled.

6.10.15 PME Event Enable 1 Register — Index F0h

Bit	Name	R/W	Reset	Default	Description
7	WDT_PME_EN	R/W	3VA	0	WDT PME event enable. 0: disable WDT PME event. 1: enable WDT PME event.
6	MO_PME_EN	R/W	3VA	0	Mouse PME event enable. 0: disable mouse PME event. 1: enable mouse PME event.
5	KB_PME_EN	R/W	3VA	0	Keyboard PME event enable. 0: disable keyboard PME event. 1: enable keyboard PME event.
4	HM_PME_EN	R/W	3VA	0	Hardware monitor PME event enable. 0: disable hardware monitor PME event. 1: enable hardware monitor PME event.
3	Reserved	-	-	-	Reserved.
2	UR2_PME_EN	R/W	3VA	0	UART 2 PME event enable. 0: disable UART 2 PME event. 1: enable UART 2 PME event.
1	UR1_PME_EN	R/W	3VA	0	UART 1 PME event enable. 0: disable UART 1 PME event. 1: enable UART 1 PME event.
0	Reserved	-	-	-	Reserved.

6.10.16 PME Event Status 1 Register — Index F1h

Bit	Name	R/W	Reset	Default	Description
7	WDT_PME_ST	R/WC	3VA	-	WDT PME event status. 0: WDT has no PME event. 1: WDT has a PME event to assert. Write 1 to clear to be ready for next PME event.
6	MO_PME_ST	R/WC	3VA	-	Mouse PME event status. 0: Mouse has no PME event. 1: Mouse has a PME event to assert. Write 1 to clear to be ready for next PME event.
5	KB_PME_ST	R/WC	3VA	-	Keyboard PME event status. 0: Keyboard has no PME event. 1: Keyboard has a PME event to assert. Write 1 to clear to be ready for next PME event.
4	HM_PME_ST	R/WC	3VA	-	Hardware monitors PME event status. 0: Hardware monitor has no PME event. 1: Hardware monitor has a PME event to assert. Write 1 to clear to be ready for next PME event.
3	Reserved	-	-	-	Reserved.
2	UR2_PME_ST	R/WC	3VA	-	UART 2 PME event status. 0: UART 2 has no PME event. 1: UART 2 has a PME event to assert. Write 1 to clear to be ready for next PME event.

1	UR1_PME_ST	R/WC	3VA	-	UART 1 PME event status. 0: UART 1 has no PME event. 1: UART 1 has a PME event to assert. Write 1 to clear to be ready for next PME event.
0	Reserved	-	-	-	Reserved.

6.10.17 PME Event Enable 2 Register — Index F2h

Bit	Name	R/W	Reset	Default	Description
7-3	Reserved	-	-	-	Reserved.
2	RI2_PME_EN	R/W	3VA	0	RI2# PME event enable. 0: disable RI2# PME event. 1: enable RI2# PME event.
1	RI1_PME_EN	R/W	3VA	0	RI1# PME event enable. 0: disable RI1# PME event. 1: enable RI1# PME event.
0	GPIO_PME_EN	R/W	3VA	0	GPIO PME event enable. 0: disable GPIO PME event. 1: enable GPIO PME event.

6.10.18 PME Event Status 2 Register — Index F3h

Bit	Name	R/W	Reset	Default	Description
7-4	Reserved	-	-	-	Reserved.
3	ERP_PME_ST	R/WC	3VA	-	ERP PME event status. 0: ERP has no PME event. 1: ERP has a PME event to assert. Write 1 to clear to be ready for next PME event.
2	RI2_PME_ST	R/WC	3VA	-	RI2# PME event status. 0: RI2# has no PME event. 1: RI2# has a PME event to assert. Write 1 to clear to be ready for next PME event.
1	RI1_PME_ST	R/WC	3VA	-	RI1# PME event status. 0: RI1# has no PME event. 1: RI1# has a PME event to assert. Write 1 to clear to be ready for next PME event.
0	GP_PME_ST	R/WC	3VA	-	GPIO PME event status. 0: GPIO has no PME event. 1: GPIO has a PME event to assert. Write 1 to clear to be ready for next PME event.

6.10.19 ACPI Control Register 1 — Index F4h

Bit	Name	R/W	Reset	Default	Description
7	TS3	R/W	VBAT	0	Reserved for Fintek Internal Used.
6	LAST_ST_MODE	R/W	VBAT	0	0: Last state is sampled by PWOK and RSMRST#. 1: Last state is sampled 1 second before AC lost.
5	EN_GPWAKEUP	R/W	VBAT	0	Set one to enable GPIO wakeup event asserted via PSOUT#.

4	EN_KBWAKEUP	R/W	VBAT	0	Set one to enable keyboard wakeup event asserted via PSOUT#.
3	EN_MOWAKEUP	R/W	VBAT	0	Set one to enable mouse wakeup event asserted via PSOUT#.
2-1	PWRCTRL	R/W	VBAT	11	The ACPI Control the PS_ON# to always on or always off or keep last state 00 : keep last state 10 : Always on 01 : Bypass mode. 11: Always off
0	VSB_PWR_LOSS	R/WC	3VA	1	When 3VA power lost, it will set to 1, and write 1 to clear it

6.10.20 ACPI Control Register 2 — Index F5h

Bit	Name	R/W	Reset	Default	Description
7-6	PWOK_DELAY	R/W	VBAT	10b	The additional PWOK delay. 00: no delay 01: 100ms. 10: 200ms (default) 11: 400ms.
5	Reserved	-	-	-	Reserved.
4-3	VDD_DELAY	R/W	3VA	01b	The PWOK delay timing from 3VCCOK by followed setting 00 : 100ms 01 : 200ms (default) 10 : 300ms 11 : 400ms
2	Reserved	-	-	-	Reserved.
1	LRESET_DB_EN	R/W	3VA	0	Enable the LRESET# de-bounce. (200us)
0	WDT_DEF_DIS	R/W	3VA	0	0: WDT enable is determined by power on strap. 1: WDT default disabled.

6.10.21 ACPI Control Register 3 — Index F6h

Bit	Name	R/W	Reset	Default	Description
7	S3_SEL	R/W	3VA	0	Select the KBC S3 condition source. 0: Enter S3 state when internal 3VCCOK signal is de-asserted. 1: Enter S3 state when S3# is low or the TS3 register is set to 1.
6	PS_ON_DEL_EN	R/W	3VA	0	0: PS_ON# is the inverted of S3# signal. 1: PS_ON# will sink low only if the time after the last turn-off elapse at least 4 seconds.
5	OVP_KBRST_EN	R/W	3VA	0	Set “1” to force KBRST# low when OVP/UVP occurs.
4-0	Reserved	-	-	-	Reserved.

6.10.22 ACPI Control Register 4 — Index F7h

Bit	Name	R/W	Reset	Default	Description
7-6	Reserved	-	-	-	Reserved.
5	VCORE_S3_ON	R/W	VBAT	0	0: VCORE_EN is low in S3 state. 1: VCORE_EN is high is S3 state.

4	VLDT_S3_ON	R/W	VBAT	0	0: VLDT_EN is low in S3 state. 1: VLDT_EN is high is S3 state.
3	WDT_PWOK_EN	R/W	VBAT	0	Set “1” to enable WDTRST# & assert via PWOK.
2-0	Reserved	-	-	-	Reserved.

6.10.23 LED_VCC Control Register — Index F8h

Bit	Name	R/W	Reset	Default	Description
7	LED_VCC_INV_DIS	R/W	VBAT	0	Invert LED_VCC clock output.
6	LED_VCC_DS3	R/W	VBAT	0	Enable LED_VCC deep S3 mode. LED_VCC will output 0.25Hz clock with 75% duty when enter deep S3 state.
5-4	LED_VCC_S5_MODE	R/W	VBAT	0	Select LED_VCC mode in S5 state. The mode is controlled by {LED_VCC_S5_ADD, LED_VCC_S5_MODE} 000: Sink low. 001: Tri-state. 010: 0.5Hz clock. 011: 1Hz clock. 100: 0.125Hz clock with 50% duty. 101: 0.25Hz clock with 50% duty. 110: 0.125Hz clock with 75% duty. 111: 0.25Hz clock with 75% duty.
3-2	LED_VCC_S3_MODE	R/W	VBAT	0	Select LED_VCC mode in S3 state. The mode is controlled by {LED_VCC_S3_ADD, LED_VCC_S3_MODE} 000: Sink low. 001: Tri-state. 010: 0.5Hz clock. 011: 1Hz clock. 100: 0.125Hz clock with 50% duty. 101: 0.25Hz clock with 50% duty. 110: 0.125Hz clock with 75% duty. 111: 0.25Hz clock with 75% duty.
1-0	LED_VCC_S0_MODE	R/W	VBAT	0	Select LED_VCC mode in S0 state. The mode is controlled by {LED_VCC_S0_ADD, LED_VCC_S0_MODE} 000: Sink low. 001: Tri-state. 010: 0.5Hz clock. 011: 1Hz clock. 100: 0.125Hz clock with 50% duty. 101: 0.25Hz clock with 50% duty. 110: 0.125Hz clock with 75% duty. 111: 0.25Hz clock with 75% duty.

6.10.24 LED Additional Control Register — Index FAh

Bit	Name	R/W	Reset	Default	Description
7-4	Reserved	-	-	-	Reserved.
3	LED_VCC_DRV_EN	R/W	VBAT	0	0: LED_VCC is open drain. 1: LEC_VCC is push-pull.
2	LED_VCC_S5_MODE_ADD	R/W	VBAT	0	Refer to LED_VCC_S5_MODE.
1	LED_VCC_S3_MODE_ADD	R/W	VBAT	0	Refer to LED_VCC_S3_MODE.
0	LED_VCC_S0_MODE_ADD	R/W	VBAT	0	Refer to LED_VCC_S0_MODE.

6.10.25 ACPI Control Register 5 — Index FBh

Bit	Name	R/W	Reset	Default	Description
7	PSIN_FLAG	R/W	3VA	0	This bit will set “1” when PSIN# is pressed over the time set by PSIN_DET_SEL. Write “1” to clear this bit.
6	Reserved	R/W	3VA	0	Dummy register.
5	PWOK_VDD_DIS	R/W	3VA	0	PWOK will not refer to 3VCC power good signal when this bit is set.
4	ABNORMAL_PSOUT_EN	R/W	3VA	0	When this bit is set, PWOK drop in S0 state will assert a 250ms low pulse via PSOUT# to shut down system.
3	Reserved	R/W	VBAT	0	Dummy register.
2-1	PSIN_DET_SEL	R/W	VBAT	0	Time for PSIN_FLAG. 00: 1 sec. 01: 2 sec. 10: 3 sec. 11: 4 sec.
0	PSIN_DET_EN	R/W	VBAT	0	Set “1” to enable detecting PSIN# during power on.

6.10.26 ACPI Control Register 6 — Index FCh

Bit	Name	R/W	Reset	Default	Description
7	WDT_MODE	R/W	3VA	0	0: WDT assert once, WDT will disable after asserting WDTRST#. 1: Auto reload mode, WDT is disabled by software, timer will be reload after timeout occurs.
6	OVP_DLY_MODE	R/W	3VA	0	0: Force mode has no delay. 1: Force mode has delay as alarm mode.
5-0	Reserved	-	-	-	Reserved.

6.10.27 RI# De-bounce Select Register — Index FEh

Bit	Name	R/W	Reset	Default	Description
7-5	Reserved	-	-	-	Reserved for Fintek test mode. Don’t write “1” to this register.
4-2	Reserved	-	-	-	Reserved.
1-0	RI_DB_SEL	R/W	3VA	0	Select RI de-bounce time. 00: reserved. 01: 200us. 10: 2ms. 11: 20ms.

7 Hardware Monitor

Below registers could be accessed by I2C & LPC. Please refer to the register for more detail information:

Register CR01 ~ CR03 → Configuration Registers
Register CR04 → Debug Port Temperature Select Register
Register CR06 → I2C Slave Address Register
Register CR07 → MXM Address Register
Register CR08 → TSI Address Register
Register CR09 → SMBus Master Address Register
Register CR0A ~ CR0F → PECI/MXM/TSI Control Register 1~6
Register CR10 ~ CR37 → Voltage Setting Register
Register CR40 ~ CR4F → PECI 3.0 Command and Register
Register CR50 ~ CR5F → TSI/MXM Setting Register
Register CR60 ~ CR8E → Temperature Setting Register
Register CR90 ~ CRDF → Fan Control Setting Register
→Fan1 Detail Setting CRA0 ~ CRAF
→Fan2 Detail Setting CRB0 ~ CRBF
→Fan3 Detail Setting CRC0 ~ CRCF

7.1 Configuration Registers

7.1.1 Configuration Register 1— Index 01h

Bit	Name	R/W	Reset	Default	Description
7-3	Reserved	0h	-	0	Reserved
2	POWER_DOWN	R/W	3VA	0	Hardware monitor function power down function.
1	FAN_START	R/W	3VA	1	1: enable startup of fan monitoring operations. 0: Put the part in the standby mode.
0	V_T_START	R/W	3VA	1	1: enable startup of temperature and voltage monitoring operations 0: Put the part in the standby mode.

7.1.2 Configuration Register 2 — Index 02h

Bit	Name	R/W	Reset	Default	Description
7	TSI_RST_SEL	R/W	3VA	1	0: MXM/TSI/PECI enable registers reset by LRESET#. 1: MXM/TSI/PECI enable registers reset by VDD3VOK. Affected registers are MXM_EN, TSI_EN and PECI_EN.
6	CASE_BEEP_EN	R/W	3VA	0	0: Disable case open event output via BEEP. 1: Enable case open event output via BEEP.
5-4	OVT_MODE	R/W	3VA	0	00: The OVT# will be low active level mode. 01: The OVT# will be low pulse mode. 10: The OVT# will indicate by 1Hz LED function. 11: The OVT# will indicate by (400/800HZ) BEEP output.
3	HM_S3_MON_EN	R/W	3VA	0	0: Monitor voltage/temperature in S0 state only. 1: Monitor voltage/temperature in S0/S3/S5 state.

2	CASE_SMI_EN	R/W	3VA	0	0: Disable case open event output via PME. 1: Enable case open event output via PME.
1-0	ALERT_MODE	R/W	3VA	0	00: The ALERT# will be low active level mode. 01: The ALERT# will be high active level mode. 10: The ALERT# will indicate by 1Hz LED function. 11: The ALERT# will indicate by (400/800HZ) BEEP output.

7.1.3 Configuration Register 3 — Index 03h

Bit	Name	R/W	Reset	Default	Description
7-1	Reserved	R/W	-	0	Reserved
0	CASE_STS	R/W	VBAT	0	Case open event status write 1 to clear if case open event cleared. (This bit is powered by VBAT.)

7.2 Debug Port Temperature Select Register

7.2.1 Debug Port Temperature Select Register— Index 04h

Bit	Name	R/W	Reset	Default	Description
7-4	Reserved	R/W	3VA	0	Reserved registers.
3	Reserved	-	-	-	Reserved
2-0	DPORT_TEMP_SEL	R/W	3VA	1	0h: Reserved. 1h: Diode 1 reading. 2h: Diode 2 reading. 3h: Reserved. 4h: TSI reading. 5h: MXM reading. 6h: Reserved. 7h: PECI reading.

7.2.2 DTS I/F S3 Control Register — Index 05h

Bit	Name	R/W	Reset	Default	Description
7-3	Reserved	-	-	-	Reserved
2-0	Reserved	R/W	3VA	0	Reserved registers.

7.3 I2C Address Register

7.3.1 I2C Slave Address Register — Index 06h

Bit	Name	R/W	Reset	Default	Description
7-1	I2C_ADDR	R/W	3VA	2Eh	Address sent for I2C Slave. I2C master could use this address to access hardware monitor and configuration registers.
0	Reserved	-	-	-	Reserved

7.3.2 MXM Address Register — Index 07h

Bit	Name	R/W	Reset	Default	Description
7-1	MXM_ADDR	R/W	3VA	25h	Address sent for MXM protocol.
0	Reserved	-	-	-	Reserved

7.3.3 TSI Address Register — Index 08h

Bit	Name	R/W	Reset	Default	Description
7-1	TSI_ADDR	R/W	3VA	26h	Address sent for AMD TSI protocol.
0	Reserved	-	-	-	Reserved

7.3.4 SMBus Master Address Register — Index 09h

Bit	Name	R/W	Reset	Default	Description
7-1	SMBUS_ADDR	R/W	3VA	0	Address sent by embedded SMBus master.
0	Reserved	R/W	-	0	Reserved

7.4 Digital Temperature Control Register

7.4.1 PECI/MXM/TSI Control Register 1 — Index 0Ah

Bit	Name	R/W	Reset	Default	Description
7	Reserved	-	-	-	Reserved
6	MXM_BYTE_MODE	R/W	3VA	0	0: MXM is accessed by block read protocol. 1: MXM is accessed by send byte / receive byte protocol.
5	Reserved	-	-	-	Reserved
4	MXM_EN	R/W	VDD3VOK/ LRESET#	0	0: Disable MXM access. 1: Enable MXM access.
3-2	VTT_SEL	R/W	3VA	0	PECI (VTT) voltage selection. 00: VTT is 1.23V 01: VTT is 1.13V 10: VTT is 1.00V 11: VTT is 1.00V
1	TSI_EN	R/W	VDD3VOK/ LRESET#	0	0: Disable AMD TSI access. 1: Enable AMD TSI access.
0	PECI_EN	R/W	VDD3VOK/ LRESET#	0	0: Disable PECI access. 1: Enable PECI access.

7.4.2 PECI/MXM/TSI Control Register 2 — Index 0Bh

Bit	Name	R/W	Reset	Default	Description
7-4	CPU_SEL	R/W	3VA	0	Select the Intel CPU socket number. 0000: no CPU presented. PECI host will use Ping () command to find the CPU address. 0001: CPU is in socket 0, i.e. PECI address is 0x30. 0010: CPU is in socket 0, i.e. PECI address is 0x31. 0100: CPU is in socket 0, i.e. PECI address is 0x32. 1000: CPU is in socket 0, i.e. PECI address is 0x33. Others are reserved.
3-1	Reserved	-	-	0	Reserved.
0	DOMAIN1_EN	R/W	3VA	0	If the CPU is selected as dual core. Set this register 1 to read the temperature of domain1.

7.4.3 PECI/MXM/TSI Control Register 3— Index 0Ch

Bit	Name	R/W	Reset	Default	Description
7-0	TCC_TEMP	R/W	3VA	8'h55	TCC Activation Temperature. When PECI is enabled, the absolute value of CPU temperature is calculated by the equation: CPU_TEMP = TCC_TEMP + PECI Reading. The range of this register is -128 ~ 127°C.

7.4.4 PECI/MXM/TSI Control Register 4— Index 0Dh

Bit	Name	R/W	Reset	Default	Description
7-0	TSI_OFFSET	R/W	3VA	0	This byte is used as the offset to be added to the CPU temperature reading of AMD_TSI. The range of this register is -128 ~ 127°C.

7.4.5 PECI/MXM/TSI Control Register 5 — Index 0Eh

Bit	Name	R/W	Reset	Default	Description
7-0	MXM_OFFSET	R/W	3VA	0	This byte is used as the offset to be added to the temperature reading of MXM. The range of this register is -128 ~ 127°C.

7.4.6 PECI/MXM/TSI Control Register 6— Index 0Fh

Bit	Name	R/W	Reset	Default	Description
7-2	Reserved	-	-	0	Reserved.
1-0	DIG_RATE_SEL	R/W	3VA	0	Reserved for Fintek use only

7.5 Voltage Setting

7.5.1 Voltage-Protect Shut Down Enable Register — Index 10h

Bit	Name	R/W	Reset	Default	Description
7-2	Reserved	-	-	0	Reserved.

1	V1_PME_EN	R/W	3VA	0	VIN1 (Vcore) PME# event enable.
0	VCC_VP_EN	R/W	VBAT*	0	Voltage-Protect shut down enable for 3VCC

*OVP Enable bit is auto clear when OVP event occurs if OVP_MODE is “1” and ALARM_RESET_DIS is “0”

7.5.2 Voltage-Protect Status Register — Index 11h

Bit	Name	R/W	Reset	Default	Description
7-2	Reserved	-	-	0	Reserved.
1	V1_EXC_STS	R/WC	VBAT/ 3VA*	0	This bit is set when V1_EXC is changed. Write “1” to clear this bit.
0	V_EXC_VP	R/WC	VBAT/ 3VA*	0	This bit is voltage-protect status. Once 3VCC over its over-voltage limits or under its under-voltage limits and if the voltage-protect shut down enable bit is set, this bit will be set to 1. Write a 1 to this bit will clear it to 0. (This bit is powered by VBAT)

*Reset by VBAT when OVP_MODE is “0”, Reset by 3VA when OVP_MODE is “1”

7.5.3 VIN1 Over Limit Register (Powered by VBAT) — Index 12h

Bit	Name	R/W	Reset	Default	Description
7-2	Reserved	-	-	0	Reserved.
1	V1_EXC	R/WC	3VCC*	0	VIN1 over limit real time status. It is set when VIN1 is over V1_HIGH_LIMIT and clear when VIN1 is under V1_HIGH_LIMIT.
0	Reserved	-	-	0	Reserved.

7.5.4 Voltage-Protect Configuration Register — Index 16h

Bit	Name	R/W	Reset	Default	Description
7-4	Reserved	-	-	-	Reserved.
3-2	PU_TIME	R/W	VBAT	2’h1	PS_ON# de-active time select in alarm mode of voltage protection. 00: PS_ON# tri-state 0.5 sec and then inverted of S3# when over voltage or under voltage occurred. 01: PS_ON# tri-state 1 sec and then inverted of S3# when over voltage or under voltage occurred. 10: PS_ON# tri-state 2 sec and then inverted of S3# when over voltage or under voltage occurred. 11: PS_ON# tri-state 4 sec and then inverted of S3# when over voltage or under voltage occurred.
1-0	VP_EN_DELAY	R/W	VBAT	2’h2	VP_EN_DELAY could set the delay time to start voltage protecting after VDD power is ok when OVP_MODE is 1. 00: bypass 01: 50ms 10: 100ms 11: 200ms

7.5.5 VIN1 Offset Register — Index 3Eh

Bit	Name	R/W	Reset	Default	Description
7-0	V1_OFFSET	R/W	3VA	0	This byte is added to VIN1 reading to present the value in index 0x21. The notation is 2's complement.

7.5.6 Voltage Protection Power Good Select Register — Index 3Fh

Bit	Name	R/W	Reset	Default	Description
7-1	Reserved	--	-	0	Reserved
0	OVP_RST_SEL	R/W	VBAT	0	0: OVP/UVP power good signal is 3VCCOK (3VCC > 2.8V) 1: OVP/UVP power good signal is PWOK. OVP/UVP function wont' start detecting until power good.

7.5.7 Voltage reading and limit— Index 20h- 3Ah

Address	Attribute	Reset	Default Value	Description
20h	R	3VCC	--	3VCC reading. The unit of reading is 8mV.
21h	R	3VCC	--	VIN1 (Vcore) reading. The unit of reading is 8mV.
22h	R	3VCC	--	VIN2 reading. The unit of reading is 8mV.
23h~26h	R	3VCC	--	Reseved.
27h	R	3VCC	--	3VSB reading. The unit of reading is 8mV.
28h	R	3VCC	--	VBAT reading. The unit of reading is 8mV.
29h	R	3VCC	--	5VA reading. The unit of reading is 8 mV. The 5VA voltage to be monitored is internally divided by 3.
2Ah	R	3VCC	--	3VA reading. The unit of reading is 8mV.
2Bh~2Dh	R	--	--	Reserved
2Eh	R	3VCC	--	FAN2 present fan duty reading
2Fh	R	3VCC	--	FAN1 present fan duty reading
30h	R/W	VBAT	89	3VCC under-voltage protection limit. The unit is 8mV
31h	R/W	VBAT	F2	3VCC over-voltage protection limit. The unit is 8mV
32h	R/W	3VA	FF	VIN1 high limit. The unit is 8mv.
32~39h	R		FF	Reserved

7.6 PECI 3.0 Command and Register

7.6.1 PECI Configuration Register — Index 40h

Bit	Name	R/W	Reset	Default	Description
7	RDIAMSR_CMD_EN	R/W	3VA	0	When PECI temperature monitoring is enabled, set this bit 1 will generate a RdIAMSR() command before a GetTemp() command.
6	C3_UPDATE_EN	R/W	3VA	1	If RDIAMSR_CMD_EN is not set to 1, the temperature data is not allowed to be updated when the completion code of RdIAMSR() is 0x82.
5-4	Reserved	R	-	-	Reserved
3	C3_PTEMP_EN	R/W	3VA	0	Set this bit 1 to enable updating positive value of temperature if the completion code of RdIAMSR() is 0x82.

2	C0_PTEMP_EN	R/W	3VA	1	Set this bit 1 to enable updating positive value of temperature if the completion code of RdIAMSR() is not 0x82 and the bit 8 of completion code is not 1 either.
1	C3_ALL0_EN	R/W	3VA	0	Set this bit 1 to enable updating temperature value 0x0000 if the completion code of RdIAMSR() is 0x82.
0	C0_ALL0_EN	R/W	3VA	0	Set this bit 1 to enable updating temperature value 0x0000 if the completion code of RdIAMSR() is not 0x82 and the bit 8 of completion code is not 1 either.

7.6.2 PECI Master Control Register — Index 41h

Bit	Name	R/W	Reset	Default	Description
7	PECI_CMD_START	W	3VA	-	Write 1 to this bit to start a PECI command when using as a PECI master. (PECI_PENDING must be set to 1)
6-5	Reserved	R	-	-	Reserved
4	PECI_PENDING	R/W	3VA	0	Set this bit 1 to stop monitoring PECI temperature.
3	Reserved	R	-	-	Reserved
2-0	PECI_CMD	R/W	3VA	3'h0	PECI command to be used by PECI master. 000: PING() 001: GetDIB() 010: GetTemp() 011: RdIAMSR() 100: RdPkgConfig() 101: WrPkgConfig() others: Reserved

7.6.3 PECI Master Status Register — Index 42h

Bit	Name	R/W	Reset	Default	Description
7-3	Reserved	R	-	-	Reserved
2	ABORT_FCS	R/WC	3VA	-	This bit is the Abort FCS status of PECI master commands. Write this bit 1 or read this byte will clear this bit to 0.
1	PECI_FCS_ERR	R/WC	3VA	-	This bit is the FCS error status of PECI master commands. Write this bit 1 or read this byte will clear this bit to 0.
0	PECI_FINISH	R/WC	3VA	-	This bit is the Command Finish status of PECI master commands. Write this bit 1 or read this byte will clear this bit to 0.

7.6.4 PECI Master DATA0 Register — Index 43h

Bit	Name	R/W	Reset	Default	Description
7-0	PECI_DATA0	R/W	3VA	0	For RdIAMSR(), RdPkgConfig() and WrPkgConfig() command, this byte represents "Host ID[7:1] & Retry[0]". Please refer to PECI interface specification for more detail.

7.6.5 PECI Master DATA1 Register — Index 44h

Bit	Name	R/W	Reset	Default	Description

7-0	PECI_DATA1	R/W	3VA	0	For RdIAMSR() , this byte represents “Processor ID”. For RdPkgConfig() and WrPkgConfig() , this byte represents “Index”. Please refer to PECI interface specification for more detail.

7.6.6 PECI Master DATA2 Register — Index 45h

Bit	Name	R/W	Reset	Default	Description
7-0	PECI_DATA2	R/W	3VA	0	For RdIAMSR(), this byte is the least significant byte of “MSR Address”. For RdPkgConfig() and WrPkgConfig(), this byte is the least significant byte of “Parameter”. Please refer to PECI interface specification for more detail.

7.6.7 PECI Master DATA3 Register — Index 46h

Bit	Name	R/W	Reset	Default	Description
7-0	PECI_DATA3	R/W	3VA	0	For RdIAMSR(), this byte is the most significant byte of “MSR Address”. For RdPkgConfig() and WrPkgConfig(), this byte is the most significant byte of “Parameter”. Please refer to PECI interface specification for more detail.

7.6.8 PECI Master DATA4 Register — Index 47h

Bit	Name	R/W	Reset	Default	Description
7-0	PECI_DATA4	R/W	3VA	0	For GetDIB() , this byte represents “Device Info” For GetTemp(), this byte represents the least significant byte of temperature. For RdIAMSR() and RdPkgConfig() , this byte is “Completion Code”. For WrPkgConfig(), this byte represents “DATA[7:0]”

7.6.9 PECI Master DATA5 Register — Index 48h

Bit	Name	R/W	Reset	Default	Description
7-0	PECI_DATA5	R/W	3VA	0	For GetDIB() , this byte represents “Revision Number” For GetTemp(), this byte represents the most significant byte of temperature. For RdIAMSR() and RdPkgConfig() , this byte represents “DATA[7:0]” For WrPkgConfig(), this byte represents “DATA[15:8]”

7.6.10 PECI Master DATA6 Register — Index 49h

Bit	Name	R/W	Reset	Default	Description
7-0	PECI_DATA6	R/W	3VA	0	For RdIAMSR() and RdPkgConfig() , this byte represents “DATA[15:8]”. For WrPkgConfig(), this byte represents “DATA[23:16]”

7.6.11 PECI Master DATA7 Register — Index 4Ah

Bit	Name	R/W	Reset	Default	Description

7-0	PECI_DATA7	R/W	3VA	0	For RdIAMSR() and RdPkgConfig() , this byte represents "DATA[23:16]". For WrPkgConfig(), this byte represents "DATA[31:24]"

7.6.12 PECI Master DATA8 Register — Index 4Bh

Bit	Name	R/W	Reset	Default	Description
7-0	PECI_DATA8	R/W	3VA	0	For RdIAMSR() and RdPkgConfig() , this byte represents "DATA[31:24]". For WrPkgConfig(), this byte represents "AW FCS"

7.6.13 PECI Master DATA9 Register — Index 4Ch

Bit	Name	R/W	Reset	Default	Description
7-0	PECI_DATA9	R/W	3VA	0	For RdIAMSR(), this byte represents "DATA[39:32]". For WrPkgConfig(), this byte represents "Completion Code"

7.6.14 PECI Master DATA10 Register — Index 4Dh

Bit	Name	R/W	Reset	Default	Description
7-0	PECI_DATA10	R/W	3VA	0	For RdIAMSR(), this byte represents "DATA[47:40]".

7.6.15 PECI Master DATA11 Register — Index 4Eh

Bit	Name	R/W	Reset	Default	Description
7-0	PECI_DATA11	R/W	3VA	0	For RdIAMSR(), this byte represents "DATA[55:48]".

7.6.16 PECI Master DATA12 Register — Index 4Fh

Bit	Name	R/W	Reset	Default	Description
7-0	PECI_DATA12	R/W	3VA	0	For RdIAMSR(), this byte represents "DATA[63:56]".

7.7 TSI/MXM Temperature Setting

7.7.1 TSI Temperature – Index 50h

Bit	Name	R/W	Reset	Default	Description
7-0	TSI_TEMP	R/W	3VA	-	This is the AMD TSI temperature reading.

7.7.2 MXM Temperature 0 – Index 51h

Bit	Name	R/W	Reset	Default	Description
7-0	MXM_TEMP0	R/W	3VA	-	This is the high byte of MXM temperature reading. The raw MXM temperature is determined by: MXM_BYTE_MODE is "0", it is {MXM_TEMP0[0],MXM_TEMP1[7:1]}. MXM_BYTE_MODE is "1", it is MXM_TEMP0[7:0].

7.7.3 MXM Temperature 1 – Index 52h

Bit	Name	R/W	Reset	Default	Description
7-0	MXM_TEMP1	R/W	3VA	-	This is the low byte of MXM temperature reading. This byte is not used if MXM_BYTE_MODE is “1”.

7.7.4 MXM Index – Index 53h

Bit	Name	R/W	Reset	Default	Description
7-0	MXM_TEMP_IDX	R/W	3VA	3h	This byte is used for 1. Command sent for MXM protocol if MXM_BYTE_MODE is “0”. 2. Index sent for MXM protocol if MXM_BYTE_MODE is “1”.

7.7.5 SMBus Data 0 – Index 54h

Bit	Name	R/W	Reset	Default	Description
7-0	SMBUS_DATA0	R/W	3VA	8’h00	This is the first byte of the block read/write protocol.

7.7.6 SMBus Data 1 – Index 55h

Bit	Name	R/W	Reset	Default	Description
7-0	SMBUS_DATA1	R/W	3VA	8’h00	This is the second byte of the block read/write protocol.

7.7.7 SMBus Data 2 – Index 56h

Bit	Name	R/W	Reset	Default	Description
7-0	SMBUS_DATA2	R/W	3VA	8’h00	This is the third byte of the block read/write protocol.

7.7.8 SMBus Data 3 – Index 57h

Bit	Name	R/W	Reset	Default	Description
7-0	SMBUS_DATA3	R/W	3VA	8’h00	This is the 4th byte of the block read/write protocol.

7.7.9 SMBus Data 4 – Index 58h

Bit	Name	R/W	Reset	Default	Description
7-0	SMBUS_DATA4	R/W	3VA	8’h00	This is the 5th byte of the block read/write protocol.

7.7.10 SMBus Data 5 – Index 59h

Bit	Name	R/W	Reset	Default	Description
7-0	SMBUS_DATA5	R/W	3VA	8’h00	This is the 6th byte of the block read/write protocol.

7.7.11 SMBus Data 6 – Index 5Ah

Bit	Name	R/W	Reset	Default	Description
7-0	SMBUS_DATA6	R/W	3VA	8’h00	This is the 7th byte of the block read/write protocol.

7.7.12 SMBus Data 7 – Index 5Bh

Bit	Name	R/W	Reset	Default	Description
7-0	SMBUS_DATA7	R/W	3VA	8'h00	This is the 8th byte of the block read/write protocol.

7.7.13 Block Write Count Register – Index 5Ch

Bit	Name	R/W	Reset	Default	Description
7-4	Reserved	-	-	0	Reserved
3-0	BLOCK_WR_CNT	R/W	3VA	0	Use the register to specify the byte count of block write protocol. Support up to 10 bytes.

7.7.14 SMBUS Command Byte/TSI Command Byte – Index 5Dh

Bit	Name	R/W	Reset	Default	Description
7-0	SMBUS_CMD/TSI_CMD	R/W	3VA	0/1	There are actual two bytes for this index. TSI_CMD_PROG select which byte to be programmed: 0: SMBUS_CMD, which is the command code for write byte/word, read byte/word, block write/read and process call protocol. 1: TSI_CMD, which is the command code for Intel temperature interface block read protocol and the data byte for AMD TSI send byte protocol.

7.7.15 SMBUS Status – Index 5Eh

Bit	Name	R/W	Reset	Default	Description
7	ADC_PENDING	R/W	3VA	0	Set 1 to pending auto TSI/MXM accessing. To use the SCL/ SDA as SMBUS master, set this bit to "1" first.
6	TSI_CMD_PROG	R/W	3VA	0	Set 1 to program TSI_CMD.
5	PROC_KILL	R/W	3VA	0	Kill the current SMBUS transfer and return the state machine to idle. It will set a fail status if the current transfer is not completed.
4	FAIL_STS	R	3VA	0	This is set when PROC_KI LL kill an un-completed transfer. It will be auto cleared by next SMBUS transfer.
3	SMBUS_ABT_ERR	R	3VA	0	This is the arbitration lost status if SMBUS command is issued. Auto cleared by next SMBUS command.
2	SMBUS_TO_ERR	R	3VA	0	This is the timeout status if SMBUS command is issued. Auto cleared by next SMBUS command.
1	SMBUS_NAC_ERR	R	3VA	0	This is the NACK error status if SMBUS command is issued. Auto cleared by next SMBUS command.
0	SMBUS_ READY	R	3VA	1	0: SMBUS transfer is in process. 1: Ready for next SMBUS command.

7.7.16 SMBUS Protocol Select – Index 5Fh

Bit	Name	R/W	Reset	Default	Description
7	SMBUS_START	W	-	0	Write "1" to trigger SMBUS transfer with the protocol specified by SMBUS_PROTOCOL.
6-4	Reserved	-	-	-	Reserved.

3-0	SMBUS_PROTOCOL	R/W	3VA	0	Select what protocol if SMBUS transfer is triggered. 0001b: send byte. 0010b: write byte. 0011b: write word. 0100b: Reserved. 0101b: block write. 0111b: quick command (write). 1001b: receive byte. 1010b: read byte. 1011b: read word. 1101b: block read. 1111b: Reserved Otherwise: reserved.

7.8 Temperature Register

7.8.1 Temperature PME# Enable Register — Index 60h

Bit	Name	R/W	Reset	Default	Description
7	Reserved	-	-	-	Reserved
6	EN_ T2_OVT_PME	R/W	3VA	0	If set this bit to 1, PME# signal will be issued when TEMP2 exceeds OVT setting.
5	EN_ T1_OVT_PME	R/W	3VA	0	If set this bit to 1, PME# signal will be issued when TEMP1 exceeds OVT setting.
4-3	Reserved	-	-	-	Reserved
2	EN_ T2_EXC_PME	R/W	3VA	0	If set this bit to 1, PME# signal will be issued when TEMP2 exceeds high limit setting.
1	EN_ T1_EXC_PME	R/W	3VA	0	If set this bit to 1, PME# signal will be issued when TEMP1 exceeds high limit setting.
0	Reserved	-	-	-	Reserved

7.8.2 Temperature Interrupt Status Register — Index 61h

Bit	Name	R/W	Reset	Default	Description
7	Reserved	-	-	-	Reserved
6	T2_OVT _STS	R/WC	3VCC	0	This bit gets 1 to indicate TEMP2 temperature sensor has exceeded OVT limit or below the “OVT limit –hysteresis”. Write 1 to clear this bit, write 0 to ignore.
5	T1_OVT _STS	R/WC	3VCC	0	This bit gets 1 to indicate TEMP1 temperature sensor has exceeded OVT limit or below the “OVT limit –hysteresis”. Write 1 to clear this bit, write 0 to ignore.
4-3	Reserved	-	-	-	Reserved
2	T2_EXC _STS	R/WC	3VCC	0	This bit gets 1 to indicate TEMP2 temperature sensor has exceeded high limit or below the “high limit –hysteresis” limit. Write 1 to clear this bit, write 0 to ignore.
1	T1_EXC _STS	R/WC	3VCC	0	This bit gets 1 to indicate TEMP1 temperature sensor has exceeded high limit or below the “high limit –hysteresis” limit. Write 1 to clear this bit, write 0 to ignore.

0	Reserved	-	-	-	Reserved

7.8.3 Temperature Real Time Status Register — Index 62h

Bit	Name	R/W	Reset	Default	Description
7	Reserved	-	-	-	Reserved
6	T2_OVT	R	3VCC	0	Set when the TEMP2 exceeds the OVT limit. Clear when the TEMP2 is below the “OVT limit –hysteresis” temperature.
5	T1_OVT	R	3VCC	0	Set when the TEMP1 exceeds the OVT limit. Clear when the TEMP1 is below the “OVT limit –hysteresis” temperature.
4-3	Reserved	-	-	-	Reserved
2	T2_EXC	R	3VCC	0	Set when the TEMP2 exceeds the high limit. Clear when the TEMP2 is below the “high limit –hysteresis” temperature.
1	T1_EXC	R	3VCC	0	Set when the TEMP1 exceeds the high limit. Clear when the TEMP1 is below the “high limit –hysteresis” temperature.
0	Reserved	-	-	-	Reserved

7.8.4 T1 OVT and High Limit Temperature Select Register — Index 64h

Bit	Name	R/W	Reset	Default	Description
7-6	Reserved	-	-	0	Reserved
5-4	OVT_TEMP_SEL	R/W	3VA	0	Select the source temperature for T1 OVT Limit. 0: Select T1 to be compared to Temperature 1 OVT Limit. 1: Select CPU temperature from PECI to be compared to Temperature 1 OVT Limit. 2: Select CPU temperature from AMD TSI or Intel PCH SMBUS to be compared to Temperature 1 OVT Limit. 3: Select the MAX temperature from Intel PCH SMBUS to be compared to Temperature 1 OVT Limit.
3-2	Reserved	-	-	0	Reserved
1-0	HIGH_ TEMP_SEL	R/W	3VA	0	Select the source temperature for T1 High Limit. 0: Select T1 to be compared to Temperature 1 High Limit. 1: Select CPU temperature from PECI to be compared to Temperature 1 High Limit. 2: Select CPU temperature from AMD TSI or Intel PCH SMBUS to be compared to Temperature 1 High Limit. 3: Select the MAX temperature from Intel PCH SMBUS to be compared to Temperature 1 High Limit.

7.8.5 OVT and Alert Output Enable Register 1 — Index 66h

Bit	Name	R/W	Reset	Default	Description
7	Reserved	-	-	-	Reserved
6	EN_T2_ALERT	R/W	3VA	0	Enable temperature 2 alert event (asserted when temperature over high limit)
5	EN_T1_ALERT	R/W	3VA	0	Enable temperature 1 alert event (asserted when temperature over high limit)
4-3	Reserved	-	-	-	Reserved.
2	EN_T2_OVT	R/W	3VA	0	Enable over temperature (OVT) mechanism of temperature2.

1	EN_T1_OVT	R/W	3VA	0	Enable over temperature (OVT) mechanism of temperature1.
0	Reserved	-	-	-	Reserved.

7.8.6 Temperature Sensor Type Register — Index 6Bh

Bit	Name	R/W	Reset	Default	Description
7-3	Reserved	RO	-	0	Reserved
2	T2_MODE	R/W	3VA	1	0: TEMP2 is connected to a thermistor. 1: TEMP2 is connected to a BJT. (default)
1	T1_MODE	R/W	3VA	1	0: TEMP1 is connected to a thermistor 1: TEMP1 is connected to a BJT.(default)
0	Reserved	-	-	-	Reserved

7.8.7 TEMP1 Limit Hystersis Select Register — Index 6Ch

Bit	Name	R/W	Reset	Default	Description
7-4	TEMP1_HYS	R/W	3VA	4h	Limit hysteresis. (0~15°C) Temperature and below the (boundary – hysteresis).
3-0	Reserved	-	-	-	Reserved

7.8.8 TEMP2 and TEMP3 Limit Hystersis Select Register — Index 6Dh

Bit	Name	R/W	Reset	Default	Description
7-4	Reserved	-	-	-	Reserved
3-0	TEMP2_HYS	R/W	3VA	4h	Limit hysteresis. (0~15°C) Temperature and below the (boundary – hysteresis).

7.8.9 DIODE OPEN Status Register — Index 6Fh

Bit	Name	R/W	Reset	Default	Description
7	Reserved	-	-	-	Reserved
6	MXM_OPEN	R	3VCC	-	When MXM interface is enabled, “1” indicates the error of receiving NACK bit or a timeout occurred.
5	PECI_OPEN	R	3VCC	-	When PECI interface is enabled, “1” indicates an error code (0x0080 or 0x0081) is received from PECI slave.
4	TSI_OPEN	R	3VCC	-	When TSI interface is enabled, “1” indicates the error of receiving NACK bit or a timeout occurred.
3	Reserved	-	-	-	Reserved
2	T2_DIODE_OPEN	R	3VCC	-	“1” indicates external diode 2 is open or short
1	T1_DIODE_OPEN	R	3VCC	-	“1” indicates external diode 1 is open or short
0	Reserved	-	-	-	Reserved

7.8.10 Temperature — Index 70h- 8Dh

Address	Attribute	Reset	Default Value	Description
70h	Reserved	--	--	Reserved
71h	Reserved	--	--	Reserved

72h	R	3VCC/ 3VA	--	Temperature 1 reading. The unit of reading is 1°C.At the moment of reading this register.
73h	Reserved	--	--	Reserved
74h	R	3VCC/ 3VA	--	Temperature 2 reading. The unit of reading is 1°C.At the moment of reading this register.
75h~79h	Reserved	--	--	Reserved
7Ah	R	3VCC/ 3VA	--	The data of CPU temperature from digital interface after IIR filter. (Available if AMD TSI interface is enabled)
7Bh	R	3VCC/ 3VA	--	The data of MXM temperature from digital interface after IIR filter. (Available if Intel MXM interface is enabled)
7Ch	R	3VCC	--	Reserved
7Dh	R	3VCC	--	Reserved
7Eh	R	3VCC/ 3VA	--	The data of CPU temperature from digital interface after IIR filter. (Available if PECI interface is enabled)
80h	R	3VCC	--	Reserved
81h	R	3VCC	--	Reserved
82h	R/W	3VA	64h	Temperature sensor 1 OVT limit. The unit is 1°C.
83h	R/W	3VA	55h	Temperature sensor 1 high limit. The unit is 1°C.
84h	R/W	3VA	64h	Temperature sensor 2 OVT limit. The unit is 1°C.
85h	R/W	3VA	55h	Temperature sensor 2 high limit. The unit is 1°C.
86-8Bh	--	--	--	Reserved
8C~8Dh	--	--	--	Reserved

7.8.11 T1 Slope Adjust Register — Index 7Fh

<table>
<tr><th>Bit</th><th>Name</th><th>R/W</th><th>Reset</th><th>Default</th><th colspan="3">Description</th></tr>
<tr><td>7-4</td><td>Reserved</td><td>-</td><td>-</td><td>-</td><td colspan="3">Reserved</td></tr>
<tr><td>3</td><td>T1_ADD</td><td>R/W</td><td>3VA</td><td>0h</td><td colspan="3">This bit is the sign bit for T1 reading slope adjustment. See T1_SCALE below for detail.</td></tr>
<tr><td>2</td><td>Reserved</td><td>-</td><td>-</td><td>-</td><td colspan="3">Reserved</td></tr>
<tr><td rowspan="9">1-0</td><td rowspan="9">T1_SCALE</td><td rowspan="9">R/W</td><td rowspan="9">3VA</td><td rowspan="9">0h</td><td colspan="3"></td></tr>
<tr><td>T1_ADD</td><td>T1_SCALE</td><td>Slope</td></tr>
<tr><td>X</td><td>00</td><td>No adjustment</td></tr>
<tr><td>0</td><td>01</td><td>15/16</td></tr>
<tr><td>0</td><td>10</td><td>31/32</td></tr>
<tr><td>0</td><td>11</td><td>63/64</td></tr>
<tr><td>1</td><td>01</td><td>17/16</td></tr>
<tr><td>1</td><td>10</td><td>33/32</td></tr>
<tr><td>1</td><td>11</td><td>65/64</td></tr>
</table>

7.8.12 Temperature Filter Select Register — Index 8Eh

Bit	Name	R/W	Reset	Default	Description
7-6	Reserved	-	-	-	Reserved
5-4	IIR-QUEUR2	R/W	3VA	2'b10	The queue time for second filter to quickly update values. 00: 8 times. 01: 12 times. 10: 16 times. (default) 11: 24 times.
3-2	IIR-QUEUR1	R/W	3VA	2'b10	The queue time for second filter to quickly update values. 00: 8 timers. 01: 12 times. 10: 16 times. (default) 11: 24 times.
1-0	IIR-QUEUR_DIG	R/W	3VA	2'b10	The queue time for second filter to quickly update values. (for CPU temperature from PECI or TSI interface) 00: 8 timers. 01: 12 times. 10: 16 times. (default) 11: 24 times.

7.9 Fan Control Setting

7.9.1 FAN PME# Enable Register — Index 90h

Bit	Name	R/W	Reset	Default	Description
7-2	Reserved	R	-	0	Reserved
1	EN_FAN2_PME	R/W	3VA	0	A one enables the corresponding interrupt status bit for PME# interrupt. Set this bit 1 to enable PME# function for Fan2.
0	EN_FAN1_PME	R/W	3VA	0	A one enables the corresponding interrupt status bit for PME# interrupt. Set this bit 1 to enable PME# function for Fan1.

7.9.2 FAN Interrupt Status Register — Index 91h

Bit	Name	R/W	Reset	Default	Description
7-2	Reserved	R	-	0	Reserved
1	FAN2_STS	R/W	3VCC	--	This bit is set when the fan2 count exceeds the count limit. Write 1 to clear this bit, write 0 will be ignored.
0	FAN1_STS	R/W	3VCC	--	This bit is set when the fan1 count exceeds the count limit. Write 1 to clear this bit, write 0 will be ignored.

7.9.3 FAN Real Time Status Register — Index 92h

Bit	Name	R/W	Reset	Default	Description
7-2	Reserved	--	-	-	Reserved
1	FAN2_EXC	R	3VCC	--	This bit set to high mean that fan2 count can't meet expect count over than SMI time (CR9F) or when duty not zero but fan stop over then 3 sec.

0	FAN1_EXC	R	3VCC	--	This bit set to high mean that fan1 count can't meet expect count over than SMI time (CR9F) or when duty not zero but fan stop over then 3 sec.

7.9.4 FAN BEEP# Enable Register — Index 93h

Bit	Name	R/W	Reset	Default	Description
7	Reserved	--	-	-	Reserved
6	FULL_WITH_ T2_EN	R/W	3VA	0	Set one will enable FAN to force full speed when T2 over high limit.
5	FULL_WITH_ T1_EN	R/W	3VA	0	Set one will enable FAN to force full speed when T1 over high limit.
4-0	Reserved	--	-	0	Reserved

7.9.5 FAN Type Select Register — Index 94h (FAN_PROG_SEL = 0)

Bit	Name	R/W	Reset	Default	Description
7-4	Reserved	--	-	0	Reserved
3-2	FAN2_TYPE	R/W	3VCC	00	00: Output PWM mode (push pull) to control fans. 01: Use linear fan application circuit to control fan speed by fan's power terminal. 10: Output PWM mode (open drain) to control Intel 4-wire fans. 11: Reserved. Bit 0 is power on trap by FANCTRL2 0: FANCTRL2 is pull up by external resistor. 1: FANCTRL2 is pull down by internal 100KΩ resistor.
1-0	FAN1_TYPE	R/W	3VCC	00	00: Output PWM mode (push pull) to control fans. 01: Use linear fan application circuit to control fan speed by fan's power terminal. 10: Output PWM mode (open drain) to control Intel 4-wire fans. 11: Reserved. Bit 0 is power on trap by FANCTRL1 0: FANCTRL1 is pull up by external resistor. 1: FANCTRL1is pull down by internal 100KΩ resistor.

S: Register default values are decided by trapping.

7.9.6 Fan1 Base Temperature Register – Index 94h (FAN_PROG_SEL = 1)

Bit	Name	R/W	Reset	Default	Description
7-0	FAN1_BASE _TEMP	R/W	3VA	0	This register is used to set the base temperature for FAN1 temperature adjustment. The FAN1 temperature is calculated according to the equation: Tfan1 = Tnow + (Ta – Tb)*Ct Where Tnow is selected by FAN1_TEMP_SEL_DIG and FAN1_TEMP_SEL. Tb is this register, Ta is selected by TFAN1_ADJ_SEL and Ct is selected by TFAN1_ADJ_UP_RATE/TFAN1_ADJ_DN_RATE. To access this register, FAN_PROG_SEL (CR9F [7]) must set to "1".

7.9.7 FAN1 Temperature Adjustment Rate Register — Index 95h (FAN_PROG_SEL = 1)

Bit	Name	R/W	Reset	Default	Description
7	Reserved	-	-	-	Reserved
6-4	TFAN1_ADJ_UP _RATE		3VA	3'h0	This selects the weighting of the difference between Ta and Tb if Ta is higher than Tb. 3'h1: 1 (Ct = 1) 3'h2: 1/2 (Ct= 1/2) 3'h3: 1/4 (Ct = 1/4) 3'h4: 1/8 (Ct = 1/8) otherwise: 0 To access this byte, FAN_PROG_SEL must set to "1".
3	Reserved	-		-	Reserved
2-0	TFAN1_ADJ_DN _RATE	R/W	3VA	3'h0	This selects the weighting of the difference between Ta and Tb if Ta is lower than Tb. 3'h1: 1 (Ct = 1) 3'h2: 1/2 (Ct= 1/2) 3'h3: 1/4 (Ct = 1/4) 3'h4: 1/8 (Ct = 1/8) otherwise: 0 To access this byte, FAN_PROG_SEL must set to "1".

7.9.8 FAN mode Select Register — Index 96h (FAN_PROG_SEL = 0)

Bit	Name	R/W	Reset	Default	Description
7-4	Reserved	--	-	0	Reserved
3-2	FAN2_MODE	R/W	VBAT	01	00: Auto fan speed control. Fan speed will follow different temperature by different **RPM** defined in 0xB6-0xBE. 01: Auto fan speed control. Fan speed will follow different temperature by different **duty cycle** (voltage) defined in 0xB6-0xBE. 10: Manual mode fan control. User can write expected **RPM** count to 0xB2-0xB3, and F81803 will adjust duty cycle (PWM fan type) or voltage (linear fan type) to control fan speed automatically. 11: Manual mode fan control, user can write expected **duty cycle** (PWM fan type) or voltage (linear fan type) to 0xB3, and F81803 will output this desired duty or voltage to control fan speed.
1-0	FAN1_MODE	R/W	VBAT	01	00: Auto fan speed control. Fan speed will follow different temperature by different **RPM** defined in 0xA6-0xAE. 01: Auto fan speed control. Fan speed will follow different temperature by different **duty cycle** defined in 0xA6-0xAE. 10: Manual mode fan control, user can write expected **RPM** count to 0xA2-0xA3, and F81803 will auto control duty cycle (PWM fan type) or voltage (linear fan type) to control fan speed automatically. 11: Manual mode fan control, user can write expected **duty cycle** (PWM fan type) or voltage (linear fan type) to 0xA3, and F81803 will output this desired duty or voltage to control fan speed.

7.9.9 FAN mode Select Register — Index 96h (FAN_PROG_SEL = 1)

Bit	Name	R/W	Reset	Default	Description
7-5	Reserved	-		-	Reserved

4	FREQ_SEL_ADD2	R/W	3VA	0	This bit and FAN2_PWM_FREQ_SEL are used to select FAN2 PWM frequency. NEW_FREQ_SEL2 = { FREQ_SEL_ADD2, FAN2_PWM_FREQ_SEL} 00: 23.5 KHz 01: 11.75 KHz 10: 5.875 KHz 11: 220 Hz
3	FREQ_SEL_ADD1	R/W	3VA	0	This bit and FAN1_PWM_FREQ_SEL are used to select FAN1 PWM frequency. NEW_FREQ_SEL1 = { FREQ_SEL_ADD1, FAN1_PWM_FREQ_SEL} 00: 23.5 KHz 01: 11.75 KHz 10: 5.875 KHz 11: 220 Hz
2-0	TFAN1_ADJ_SEL	R/W	3VA	0h	This selects which temperature to be used as Ta for Fan1 temperature adjustment. 000: PECI (CR7Eh) 001: T1 (CR72h) 010: T2 (CR74h) 011: Reserved. 100: TSI CPU temperature (CR7Ah) 101:MXM temperature (CR7Bh). 110: Resrved. 111: Resrved. otherwise: Ta will be 0. To access this register FAN_PROG_SEL must set to “1”.

7.9.10 Auto FAN1 and FAN2 Boundary Hystersis Select Register — Index 98h

Bit	Name	R/W	Reset	Default	Description
7-4	FAN2_HYS	R/W	3VA	4h	Boundary hysteresis. (0~15°C) Segment will change when the temperature over the boundary temperature and below the (boundary – hysteresis).
3-0	FAN1_HYS	R/W	3VA	4h	Boundary hysteresis. (0~15°C) Segment will change when the temperature over the boundary temperature and below the (boundary – hysteresis).

7.9.11 Auto Fan Up Speed Update Rate Select Register — Index 9Ah

Bit	Name	R/W	Reset	Default	Description
7-4	Reserved	--	-	0	Reserved
3-2	FAN2_UP_RATE	R/W	3VA	01	Fan2 duty update rate: 00: 2Hz 01: 5Hz (default) 10: 10Hz 11: 20Hz

1-0	FAN1_UP_RATE	R/W	3VA	01	Fan1 duty update rate: 00: 2Hz 01: 5Hz (default) 10: 10Hz 11: 20Hz

7.9.12 Auto Fan Down Speed update Rate Select Register — Index 9Bh (FAN_PROG_SEL = 0)

Bit	Name	R/W	Reset	Default	Description
7-4	Reserved	--	-	0	Reserved
3-2	FAN2_DN_RATE	R/W	3VA	01	Fan2 duty update rate: 00: 2Hz 01: 5Hz (default) 10: 10Hz 11: 20Hz
1-0	FAN1_DN_RATE	R/W	3VA	01	Fan1 duty update rate: 00: 2Hz 01: 5Hz (default) 10: 10Hz 11: 20Hz

7.9.13 Auto Fan Down Speed update Rate Select Register — Index 9Bh (FAN_PROG_SEL = 1)

Bit	Name	R/W	Reset	Default	Description
7	UP_DN_RATE_EN	R/W	3VA	0	0: Fan down rate disable 1: Fan down rate enable Set this bit 1 to use different fan up/down rate. If this bit is not set to 1, the fan up/down rate will follow FAN_UP_RATE.
6	DIRECT_LOAD_EN	R/W	3VA	0	0: Direct load disable 1: Direct load enable for manual duty mode
5-0	Reserved	-	-	-	Reserved

7.9.14 FAN1 and FAN2 START UP DUTY-CYCLE/VOLTAGE — Index 9Ch

Bit	Name	R/W	Reset	Default	Description
7-4	FAN2_STOP _DUTY	R/W	3VA	5h	When fan start, the FAN_CTRL2 will increase duty-cycle from 0 to this (value x 8) directly. And if fan speed is down, the FAN_CTRL 2 will decrease duty-cycle to 0 when the PWM duty cycle is less than this (value x 4).
3-0	FAN1_STOP _DUTY	R/W	3VA	5h	When fan start, the FAN_CTRL 1 will increase duty-cycle from 0 to this (value x 8 directly. And if fan speed is down, the FAN_CTRL 1 will decrease duty-cycle to 0 when the PWM duty cycle is less than this (value x 4).

7.9.15 FAN PROGRAMMABLE DUTY-CYCLE/VOLTAGE LOADED AFTER POWER-ON — Index 9Eh

Bit	Name	R/W	Reset	Default	Description

7-0	PROG_DUTY_VAL	R/W	VBAT	66h/ FFh	This byte will be immediately loaded as Fan duty value after VDD is powered on if it has been programmed before shut down. Default value is powered on strapped by FAN_40_100.

7.9.16 Fan Fault Time Register — Index 9Fh

Bit	Name	R/W	Reset	Default	Description
7	FAN_PROG_SEL	R/W	3VA	0	Set this bit to “1” will enable accessing registers of other bank.
6	FAN_MNT_SEL	R/W	3VA	0	Set this bit to monitor a slower fan.
5	Reserved	-	-	-	Reserved
4	FAN40_100_SEL	RO	3VCC	-	This bit is the power on trap value of FAN40_100.
3-0	F_FAULT_TIME	R/W	3VA	Ah	This register determines the time of fan fault. The condition to cause fan fault event is: When PWM_Duty reaches FFh, if the fan speed count can’t reach the fan expect count in time. The unit of this register is 1 second. The default value is 11 seconds. (Set to 0, means 1 seconds; Set to 1, means 2 seconds. Set to 2, means 3 seconds. ….) Another condition to cause fan fault event is fan stop and the PWM duty is greater than the minimum duty programmed by the register index 9C-9Dh.

7.10 Fan1 Detail Setting

7.10.1 FAN1 Index A0h~AFh

Address	Attribute	Reset	Default	Description
A0h	RO	3VCC	8’h0F	FAN1 count reading (MSB). At the moment of reading this register, the LSB will be latched. This will prevent from data updating when reading. To read the fan count correctly, read MSB first and followed read the LSB.
A1h	RO	3VCC	8’hFF	FAN1 count reading (LSB).
A2h	R/W	3VA	8’h00	RPM mode(CR96 bit0=0): FAN1 expect speed count value (MSB), in auto fan mode (CR96 bit1➔0) this register is auto updated by hardware. Duty mode(CR96 bit0=1): This byte is reserved byte.
A3h	R/W	3VA	8’h01	RPM mode(CR96 bit0=0): FAN1 expect speed count value (LSB) or expect PWM duty, in auto fan mode this register is auto updated by hardware and read only. Duty mode(CR96 bit0=1): The Value programming in this byte is duty value. In auto fan mode (CR96 bit1➔0) this register is updated by hardware. Ex: 5➔ 5*100/255 % 255 ➔ 100%
A4h	R/W	3VA	8’h03	FAN1 full speed count reading (MSB). At the moment of reading this register, the LSB will be latched. This will prevent from data updating when reading. To read the fan count correctly, read MSB first and followed read the LSB.
A5h	R/W	3VA	8’hFF	FAN1 full speed count reading (LSB).

7.10.2 VT1 BOUNDARY 1 TEMPERATURE – Index A6h

Bit	Name	R/W	Reset	Default	Description
7-0	BOUND1TMP1	R/W	3VA	3Ch (60°C)	The first boundary temperature for VT1 in temperature mode. When VT1 temperature **exceeds** this boundary, expected FAN1 value will be loaded from segment **1** register (index AAh). When VT1 temperature is **under** this boundary – hysteresis, expected FAN1 value will be loaded from segment **2** register (index ABh). This byte is a 2's complement value ranged from -128°C ~ 127°C.

7.10.3 VT1 BOUNDARY 2 TEMPERATURE – Index A7

Bit	Name	R/W	Reset	Default	Description
7-0	BOUND2TMP1	R/W	3VA	32 (50°C)	The 2nd BOUNDARY temperature for VT1 in temperature mode. When VT1 temperature is exceed this boundary, FAN1 expected value will load from segment 2 register (index ABh). When VT1 temperature is below this boundary – hysteresis, FAN1 expected value will load from segment 3 register (index ACh). This byte is a 2's complement value ranging from -128°C ~ 127°C.

7.10.4 VT1 BOUNDARY 3 TEMPERATURE – Index A8h

Bit	Name	R/W	Reset	Default	Description
7-0	BOUND3TMP1	R/W	3VA	28h (40°C)	The 3rd BOUNDARY temperature for VT1 in temperature mode. When VT1 temperature is exceed this boundary, FAN1 expected value will load from segment 3 register (index ACh). When VT1 temperature is below this boundary – hysteresis, FAN1 expected value will load from segment 4 register (index ADh). This byte is a 2's complement value ranging from -128°C ~ 127°C.

7.10.5 VT1 BOUNDARY 4 TEMPERATURE – Index A9

Bit	Name	R/W	Reset	Default	Description
7-0	BOUND4TMP1	R/W	3VA	1Eh (30°C)	The 4th BOUNDARY temperature for VT1 in temperature mode. When VT1 temperature is exceed this boundary, FAN1 expected value will load from segment 4 register (index ADh). When VT1 temperature is below this boundary – hysteresis, FAN1 expected value will load from segment 5 register (index AEh). This byte is a 2's complement value ranging from -128°C ~ 127°C.

7.10.6 FAN1 SEGMENT 1 SPEED COUNT – Index AAh

Bit	Name	R/W	Reset	Default	Description

7-0	SEC1SPEED1	R/W	3VA	FFh (100%)	The meaning of this register is depending on the FAN1_MODE(CR96) **2'b00:** The value that set in this byte is the relative expect fan speed % of the full speed in this temperature section. Ex: 100%:full speed: User must set this register to 0. 60% full speed: (100-60)*32/60, so user must program 21 to this reg. X% full speed: The value programming in this byte is ((100-X)*32/X 2'b01: The value that set in this byte is mean the expect PWM duty-cycle in this temperature section.

7.10.7 FAN1 SEGMENT 2 SPEED COUNT – Index ABh

Bit	Name	R/W	Reset	Default	Description
7-0	SEC2SPEED1	R/W	3VA	D9h (85%)	The meaning of this register is depending on the FAN1_MODE(CR96) 2'b00: The value that set in this byte is the relative expect fan speed % of the full speed in this temperature section. 2'b01: The value that set in this byte is mean the expect PWM duty-cycle in this temperature section.

7.10.8 FAN1 SEGMENT 3 SPEED COUNT Register – Index ACh

Bit	Name	R/W	Reset	Default	Description
7-0	SEC3SPEED1	R/W	3VA	B2h (70%)	The meaning of this register is depending on the FAN1_MODE(CR96) 2'b00: The value that set in this byte is the relative expect fan speed % of the full speed in this temperature section. 2'b01: The value that set in this byte is mean the expect PWM duty-cycle in this temperature section.

7.10.9 FAN1 SEGMENT 4 SPEED COUNT Register – Index ADh

Bit	Name	R/W	Reset	Default	Description
7-0	SEC4SPEED1	R/W	3VA	99h (60%)	The meaning of this register is depending on the FAN1_MODE(CR96) 2'b00: The value that set in this byte is the relative expect fan speed % of the full speed in this temperature section. 2'b01: The value that set in this byte is mean the expect PWM duty-cycle in this temperature section.

7.10.10 FAN1 SEGMENT 5 SPEED COUNT Register – Index AEh

Bit	Name	R/W	Reset	Default	Description
7-0	SEC5PEED1	R/W	3VA	80h (50%)	The meaning of this register is depending on the FAN1_MODE(CR96) 2'b00: The value that set in this byte is the relative expect fan speed % of the full speed in this temperature section. 2'b01: The value that set in this byte is mean the expect PWM duty-cycle in this temperature section.

7.10.11 FAN1 Temperature Mapping Select – Index AFh

Bit	Name	R/W	Reset	Default	Description

7	FAN1_TEMP _SEL_DIG	R/W	3VA	0	This bit companies with FAN1_TEMP_SEL select the temperature source for controlling FAN1.
6	FAN1_PWM _FREQ_SEL	R/W	3VA	0	This bit and FREQ_SEL_ADD1 are used to select FAN1 PWM frequency. NEW_FREQ_SEL1 = { FREQ_SEL_ADD1, FAN1_PWM_FREQ_SEL} 00: 23.5 KHz 01: 11.75 KHz 10: 5.875 KHz 11: 220 Hz
5	FAN1_UP_T_EN	R/W	3VA	0	Set 1 to force FAN1 to full speed if any temperature over its high limit.
4	FAN1_ INTERPOLATION_E N	R/W	3VA	1	Set 1 will enable the interpolation of the fan expect table.
3	FAN1_JUMP _HIGH_EN	R/W	3VA	1	This register controls the FAN1 duty movement when temperature over highest boundary. 0: The FAN1 duty will increases with the slope selected by FAN1_RATE_SEL register. 1: The FAN1 duty will directly jumps to the value of SEC1SPEED1 register. This bit only activates in duty mode.
2	FAN1_JUMP _LOW_EN	R/W	3VA	1	This register controls the FAN1 duty movement when temperature under (highest boundary – hysteresis). 0: The FAN1 duty will decreases with the slope selected by FAN1_RATE_SEL register. 1: The FAN1 duty will directly jumps to the value of SEC2SPEED1 register. This bit only activates in duty mode.
1-0	FAN1_TEMP_SEL	R/W	3VA	01	This registers company with FAN1_TEMP_SEL_DIG select the temperature source for controlling FAN1. The following value is comprised by {FAN1_TEMP_SEL_DIG, FAN1_TEMP_SEL} 000: fan1 follows PECI temperature (CR7Eh) 001: fan1 follows temperature 1 (CR72h). 010: fan1 follows temperature 2 (CR74h). 011: Reserved. 100: fan1 follows TSI CPU temperature (CR7Ah) 101: fan1 follows MXM temperature (CR7Bh). Others are reserved.

7.11 Fan2 Detail Setting

7.11.1 FAN2 Index B0h~BFh

Address	Attribute	Reset	Default Value	Description
B0h	RO	3VCC	8'h0F	FAN2 count reading (MSB). At the moment of reading this register, the LSB will be latched. This will prevent from data updating when reading. To read the fan count correctly, read MSB first and followed read the LSB.
B1h	RO	3VCC	8'hFF	FAN2 count reading (LSB).

B2h	R/W	3VA	8'h00	RPM mode(CR96 bit2=0): FAN2 expect speed count value (MSB), in auto fan mode (CR96 bit3➔0) this register is auto updated by hardware. Duty mode (CR96 bit2=1): This byte is reserved byte.
B3h	R/W	3VA	8'h01	RPM mode(CR96 bit2=0): FAN2 expect speed count value (LSB) or expect PWM duty, in auto fan mode this register is auto updated by hardware and read only. Duty mode(CR96 bit2=1): The Value programming in this byte is duty value. In auto fan mode (CR96 bit3➔0) this register is updated by hardware. Ex: 5➔ 5*100/255 % 255 ➔ 100%
B4h	R/W	3VA	8'h03	FAN2 full speed count reading (MSB). At the moment of reading this register, the LSB will be latched. This will prevent from data updating when reading. To read the fan count correctly, read MSB first and followed read the LSB.
B5h	R/W	3VA	8'hFF	FAN2 full speed count reading (LSB).

7.11.2 VT2 BOUNDARY 1 TEMPERATURE – Index B6h

Bit	Name	R/W	Reset	Default	Description
7-0	BOUND1TMP2	R/W	3VA	3Ch (60°C)	The first boundary temperature for VT2 in temperature mode. When VT2 temperature **exceeds** this boundary, FAN2 expect value will load from segment **1** register (index Bah). When VT2 temperature is **under** this boundary – hysteresis, FAN2 expect value will load from segment **2** register (index BAh). This byte is a 2's complement value ranging from -128°C ~ 127°C.

7.11.3 VT2 BOUNDARY 2 TEMPERATURE – Index B7

Bit	Name	R/W	Reset	Default	Description
7-0	BOUND2TMP2	R/W	3VA	32 (50°C)	The 2nd BOUNDARY temperature for VT2 in temperature mode. When VT2 temperature is exceed this boundary, FAN2 expected value will load from segment 2 register (index BBh). When VT2 temperature is below this boundary – hysteresis, FAN2 expected value will load from segment 3 register (index BCh). This byte is a 2's complement value ranging from -128°C ~ 127°C.

7.11.4 VT2 BOUNDARY 3 TEMPERATURE – Index B8h

Bit	Name	R/W	Reset	Default	Description
7-0	BOUND3TMP2	R/W	3VA	28h (40°C)	The 3rd BOUNDARY temperature for VT2 in temperature mode. When VT2 temperature is exceed this boundary, FAN2 expected value will load from segment 3 register (index BCh). When VT2 temperature is below this boundary – hysteresis, FAN2 expected value will load from segment 4 register (index BDh). This byte is a 2's complement value ranging from -128°C ~ 127°C.

7.11.5 VT2 BOUNDARY 4 TEMPERATURE – Index B9

Bit	Name	R/W	Reset	Default	Description
7-0	BOUND4TMP2	R/W	3VA	1Eh (30°C)	The 4th BOUNDARY temperature for VT2 in temperature mode. When VT2 temperature is exceed this boundary, FAN2 expected value will load from segment 4 register (index BDh). When VT2 temperature is below this boundary – hysteresis, FAN2 expected value will load from segment 5 register (index BEh). This byte is a 2's complement value ranging from -128°C ~ 127°C.

7.11.6 FAN2 SEGMENT 1 SPEED COUNT – Index BAh

Bit	Name	R/W	Reset	Default	Description
7-0	SEC1SPEED2	R/W	3VA	FFh (100%)	The meaning of this register is depending on the FAN2_MODE (CR96) **2'b00:** The value that set in this byte is the relative expect fan speed % of the full speed in this temperature section. Ex: 100%:full speed: User must set this register to 0. 60% full speed: (100-60)*32/60, so user must program 21 to this reg. X% full speed: The value programming in this byte is ➔ (100-X)*32/X **2'b01:** The value that set in this byte is mean the expect PWM duty-cycle in this temperature section.

7.11.7 FAN2 SEGMENT 2 SPEED COUNT – Index BBh

Bit	Name	R/W	Reset	Default	Description
7-0	SEC2SPEED2	R/W	3VA	D9h (85%)	The meaning of this register is depending on the FAN2_MODE (CR96) **2'b00:** The value that set in this byte is the relative expect fan speed % of the full speed in this temperature section. **2'b01:** The value that set in this byte is mean the expect PWM duty-cycle in this temperature section.

7.11.8 FAN2 SEGMENT 3 SPEED COUNT Register – Index BCh

Bit	Name	R/W	Reset	Default	Description
7-0	SEC3SPEED2	R/W	3VA	B2h (70%)	The meaning of this register is depending on the FAN2_MODE (CR96) **2'b00:** The value that set in this byte is the relative expect fan speed % of the full speed in this temperature section. **2'b01:** The value that set in this byte is mean the expect PWM duty-cycle in this temperature section.

7.11.9 FAN2 SEGMENT 4 SPEED COUNT Register – Index BDh

Bit	Name	R/W	Reset	Default	Description
7-0	SEC4SPEED2	R/W	3VA	99h (60%)	The meaning of this register is depending on the FAN2_MODE (CR96) **2'b00:** The value that set in this byte is the relative expect fan speed % of the full speed in this temperature section. **2'b01:** The value that set in this byte is mean the expect PWM duty-cycle in this temperature section.

7.11.10 FAN2 SEGMENT 5 SPEED COUNT Register – Index BEh

Bit	Name	R/W	Reset	Default	Description
7-0	SEC5PEED2	R/W	3VA	80h (50%)	The meaning of this register is depending on the FAN2_MODE (CR96) **2'b00:** The value that set in this byte is the relative expect fan speed % of the full speed in this temperature section. **2'b01:** The value that set in this byte is mean the expect PWM duty-cycle in this temperature section.

7.11.11 FAN2 Temperature Mapping Select – Index BFh

Bit	Name	R/W	Reset	Default	Description
7	FAN2_TEMP_ SEL_DIG	R/W	3VA	0	This bit companies with FAN2_TEMP_SEL to select the temperature source for controlling FAN2.
6	FAN2_PWM_ FREQ_SEL	R/W	3VA	0	This bit and FREQ_SEL_ADD2 are used to select FAN2 PWM frequency. NEW_FREQ_SEL2 = { FREQ_SEL_ADD2, FAN2_PWM_FREQ_SEL} 00: 23.5 KHz 01: 11.75 KHz 10: 5.875 KHz 11: 220 Hz
5	FAN2_UP_T_EN	R/W	3VA	0	Set 1 to force FAN2 to full speed if any temperature over its high limit.
4	FAN2_ INTERPOLATION_EN	R/W	3VA	1	Set 1 will enable the interpolation of the fan expect table.
3	FAN2_JUMP_ HIGH_EN	R/W	3VA	1	This register controls the FAN2 duty movement when temperature over highest boundary. 0: The FAN2 duty will increases with the slope selected by FAN2_RATE_SEL register. 1: The FAN2 duty will directly jumps to the value of SEC1SPEED2 register. This bit only activates in duty mode.
2	FAN2_JUMP_ LOW_EN	R/W	3VA	1	This register controls the FAN2 duty movement when temperature under (highest boundary – hysteresis). 0: The FAN2 duty will decreases with the slope selected by FAN2_RATE_SEL register. 1: The FAN2 duty will directly jumps to the value of SEC2SPEED2 register. This bit only activates in duty mode.
1-0	FAN2_TEMP_SEL	R/W	3VA	10	This registers companying with FAN2_TEMP_SEL_DIG select the temperature source for controlling FAN2. The following value is comprised by {FAN2_TEMP_SEL_DIG, FAN2_TEMP_SEL} 000: fan2 follows PECI temperature (CR7Eh) 001: fan2 follows temperature 1 (CR72h). 010: fan2 follows temperature 2 (CR74h). 011:Reserved. 100: fan2 follows TSI CPU temperature (CR7Ah) 101: fan2 follows MXM temperature (CR7Bh). Otherwise: reserved.

8 Electrical Characteristics

8.1 Absolute Maximum Ratings

PARAMETER	RATING	UNIT
Power Supply Voltage	-0.5 to 5.5	V
Input Voltage	-0.5 to VDD+0.5	V
Operating Temperature	-40 ~ +85*	° C
Storage Temperature	-55 to 150	° C

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may dversely affect the life and reliability of the device.

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8.2 DC Characteristics

(Ta = 0° C to 70° C, 3VCC = 3.3V ± 10%, VSS = 0V)

PARAMETER	SYM.	MIN.	TYP.	MAX.	UNIT	CONDITIONS
Operating Voltage	VDD	3.0	3.3	3.6	V	
Battery Voltage	VBAT	2.4	3.3	3.6	V	
Operating Current	ICC		10		mA	3VCC=3.3V VBAT=3.3V
Idle State Current	ISTY		5		uA	3VCC=3.3V VBAT=3.3V
Battery Current	IBAT		4		uA	3VCC=3.3V VBAT=3.3V

PARAMETER	SYM.	MIN.	TYP.	MAX.	UNIT	CONDITIONS
$I/O_{12st,5v}$-TTL level bi-directional pin with schmitt trigger, output with12 mA sink capability, 5V tolerance.						
Input Low Voltage	VIL			0.8	V	
Input High Voltage	VIH	2.0			V	
Output Low Current	IOL		+12		mA	VOL = 0.4V
Input High Leakage	ILIH			+1	μA	VIN = VDD
Input Low Leakage	ILIL	-1			μA	VIN = 0V
$I/O_{16t,u47k}$-TTL level bi-directional pin with 16 mA source-sink capability, internal pull-up 47k ohms						
Input Low Voltage	VIL			0.8	V	
Input High Voltage	VIH	2.0			V	
Output Low Current	IOL		+16		mA	VOL = 0.4V
Input High Leakage	ILIH			+1	μA	VIN = VDD
Input Low Leakage	ILIL	-1			μA	VIN = 0V
I/OOD_{12t}-TTL level bi-directional pin, Output pin with 12mA source-sink capability, and can programming to open-drain function.						
Input Low Threshold Voltage	Vt-			0.8	V	VDD = 3.3 V

Input High Threshold Voltage	Vt+	2.0			V	VDD = 3.3 V
Output Low Current	IOL		-12	-9	mA	VOL = 0.4 V
Output High Current	IOH	+9	+12		mA	VOH = 2.4V
Input High Leakage	ILIH			+1	μA	VIN = VDD
Input Low Leakage	ILIL	-1			μA	VIN = 0V
$I/OOD_{12t,5v}$-TTL level bi-directional pin, Output pin with 12mA source-sink capability, and can programming to open-drain function, 5v tolerance.						
Input Low Threshold Voltage	Vt-			0.8	V	VDD = 3.3 V
Input High Threshold Voltage	Vt+	2.0			V	VDD = 3.3 V
Output Low Current	IOL		-12	-9	mA	VOL = 0.4 V
Output High Current	IOH	+9	+12		mA	VOH = 2.4V
Input High Leakage	ILIH			+1	μA	VIN = VDD
Input Low Leakage	ILIL	-1			μA	VIN = 0V
$I/OOD_{8st,5v}$-TTL level bi-directional pin and schmitt triggrt, Open-drain output with 8mA source-sink capability, 5v tolerance.						
Input Low Threshold Voltage	Vt-			0.8	V	VDD = 3.3 V
Input High Threshold Voltage	Vt+	2.0			V	VDD = 3.3 V
Output Low Current	IOL		-8	-9	mA	VOL = 0.4 V
Output High Current	IOH	+9	+8		mA	VOH = 2.4V
Input High Leakage	ILIH			+1	μA	VIN = VDD
Input Low Leakage	ILIL	-1			μA	VIN = 0V
$I/OOD_{12st,5v}$-TTL level bi-directional pin and schmitt triggrt, Open-drain output with 12mA source-sink capability, 5v tolerance.						
Input Low Threshold Voltage	Vt-			0.8	V	VDD = 3.3 V
Input High Threshold Voltage	Vt+	2.0			V	VDD = 3.3 V
Output Low Current	IOL		-12	-9	mA	VOL = 0.4 V
Output High Current	IOH	+9	+12		mA	VOH = 2.4V
Input High Leakage	ILIH			+1	μA	VIN = VDD
Input Low Leakage	ILIL	-1			μA	VIN = 0V
$I/OOD_{24st,5v}$-TTL level bi-directional pin and schmitt triggrt, Open-drain output with 24mA source-sink capability, 5v tolerance.						
Input Low Threshold Voltage	Vt-			0.8	V	VDD = 3.3 V
Input High Threshold Voltage	Vt+	2.0			V	VDD = 3.3 V
Output Low Current	IOL		-24	-9	mA	VOL = 0.4 V
Output High Current	IOH	+9	+24		mA	VOH = 2.4V
Input High Leakage	ILIH			+1	μA	VIN = VDD
Input Low Leakage	ILIL	-1			μA	VIN = 0V
IN_{st} - TTL level input pin with schmitt trigger						
Input Low Voltage	VIL			0.8	V	
Input High Voltage	VIH	2.0			V	
Input High Leakage	ILIH			+1	μA	VIN = VDD
Input Low Leakage	ILIL	-1			μA	VIN = 0 V
$IN_{t,5v}$ - TTL level input pin with 5V tolerance.						
Input Low Voltage	VIL			0.8	V	
Input High Voltage	VIH	2.0			V	

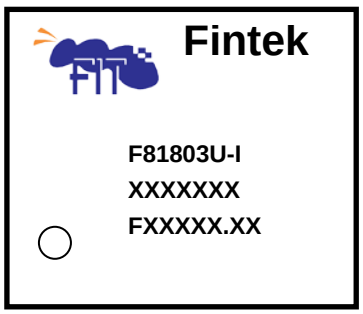
Input High Leakage	ILIH			+1	μA	VIN = VDD
Input Low Leakage	ILIL	-1			μA	VIN = 0 V
$IN_{st,5v}$ - TTL level input pin with schmitt trigger, 5V tolerance.						
Input Low Voltage	VIL			0.8	V	
Input High Voltage	VIH	2.0			V	
Input High Leakage	ILIH			+1	μA	VIN = VDD
Input Low Leakage	ILIL	-1			μA	VIN = 0 V
$IN_{st,u47k}$ - TTL level input pin with schmitt trigger, internal pull-up 47k ohms						
Input Low Voltage	VIL			0.8	V	
Input High Voltage	VIH	2.0			V	
Input High Leakage	ILIH			+1	μA	VIN = VDD
Input Low Leakage	ILIL	-1			μA	VIN = 0 V
$IN_{st,lv}$ - TTL level input pin with schmitt trigger, low level.						
Input Low Voltage	VIL			0.8	V	
Input High Voltage	VIH	2.0			V	
Input High Leakage	ILIH			+1	μA	VIN = VDD
Input Low Leakage	ILIL	-1			μA	VIN = 0 V
OD_{12}-Open-drain output with12 mA sink capability.						
Output Low Current	IOL		-12		mA	VOL = 0.4V
$OD_{12,5v}$-Open-drain output with12 mA sink capability, 5V tolerance.						
Output Low Current	IOL		-12		mA	VOL = 0.4V
$OD_{14,5v}$-Open-drain output with14 mA sink capability, 5V tolerance.						
Output Low Current	IOL		-14		mA	VOL = 0.4V
$OD_{24,5v}$-Open-drain output with24 mA sink capability, 5V tolerance.						
Output Low Current	IOL		-24		mA	VOL = 0.4V
$OD_{12,u10k,5v}$-Open-drain output with 12 mA sink capability, pull-up 10k ohms, 5V tolerance.						
Output Low Current	IOL		-12		mA	VOL = 0.4V
$OD_{16,u10k,5v}$-Open-drain output with 16 mA sink capability, pull-up 10k ohms, 5V tolerance.						
Output Low Current	IOL		-16		mA	VOL = 0.4V
$O_{8t,u47,5v}$- TTL level Output pin with 8 mA source-sink capability, pull-up 47k ohms, 5V tolerance.						
Output High Current	IOH	+6	+8		mA	VOH = 2.4V
O_{12}- Output pin with 12 mA source-sink capability.						
Output High Current	IOH	+9	+12		mA	VOH = 2.4V
O_{16}- Output pin with 16 mA source-sink capability.						
Output High Current	IOH		+16		mA	VOH = 2.4V
O_{18}- Output pin with 18 mA source-sink capability.						
Output High Current	IOH		+18		mA	VOH = 2.4V
O_{20}- Output pin with 20 mA source-sink capability.						
Output High Current	IOH		+20		mA	VOH = 2.4V
O_{30}- Output pin with 30 mA source-sink capability.						
Output High Current	IOH	+26	+30		mA	VOH = 2.4V
$O_{12,5v}$- Output pin with 12 mA source-sink capability, 5V tolerance.						
Output High Current	IOH	+9	+12		mA	VOH = 2.4V

$I_{Lv}/O_{D8,s1}$ - Low level bi-directional pin (VIH → 0.9V, VIL → 0.6V.). Output with 8mA drive and 1mA sink capability.						
Input Low Voltage	VIL			0.6	V	
Input High Voltage	VIH	0.9			V	
Output High Current	IOH		+8		mA	VOH = 1.0V
Input High Leakage	ILIH			+1	A	VIN = VDD
Input Low Leakage	ILIL	-1			A	VIN = 0 V
$I/OD_{12st,5v}$-TTL level bi-directional pin with schmitt trigger, Open-drain output with12 mA sink capability, 5V tolerance.						
Input Low Voltage	VIL			0.8	V	
Input High Voltage	VIH	2.0			V	
Output Low Current	IOL		+12		mA	VOL = 0.4V
Input High Leakage	ILIH			+1	A	VIN = VDD
Input Low Leakage	ILIL	-1			A	VIN = 0V
$I/OD_{14st,5v}$-TTL level bi-directional pin with schmitt trigger, Open-drain output with 16 mA sink capability, 5V tolerance.						
Input Low Voltage	VIL			0.8	V	
Input High Voltage	VIH	2.0			V	
Output Low Current	IOL		+14		mA	VOL = 0.4V
Input High Leakage	ILIH			+1	A	VIN = VDD
Input Low Leakage	ILIL	-1			A	VIN = 0V
$I/OD_{16st,5v}$-TTL level bi-directional pin with schmitt trigger, Open-drain output with 16 mA sink capability, 5V tolerance.						
Input Low Voltage	VIL			0.8	V	
Input High Voltage	VIH	2.0			V	
Output Low Current	IOL		+16		mA	VOL = 0.4V
Input High Leakage	ILIH			+1	A	VIN = VDD
Input Low Leakage	ILIL	-1			A	VIN = 0V
I_{Lv} /$OD_{12st,5v}$-Low level bi-directional pin with schmitt trigger, Open-drain output with12 mA sink capability, 5V tolerance.						
Input Low Voltage	VIL			0.6	V	
Input High Voltage	VIH	0.9			V	
Output Low Current	IOL		+12		mA	VOL = 0.4V
Input High Leakage	ILIH			+1	A	VIN = VDD
Input Low Leakage	ILIL	-1			A	VIN = 0V

9 Ordering Information

Part Number	Package Type
F81803U	64-TQFP (Green Package)

10 Top Marking Specification



1st Line: Fintek Logo

2nd Line: Device Name → **F81803U-I,** where U means 64-TQFP & -I means the industrial spec.

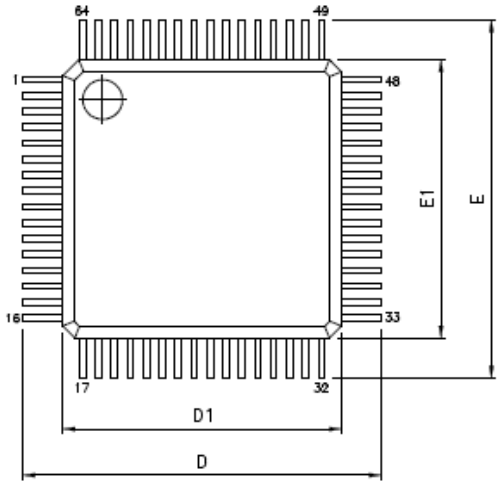
3rd Line: Assembly Plant Code (X) + Assembled Year Code (X) + Week Code (XX) + Fintek Internal Code (XX) + IC Version (X) where A means version A, B means version B, …

4th Line: Wafer Fab Code (XXXX…XX)

◯ : Pin 1 Identifier

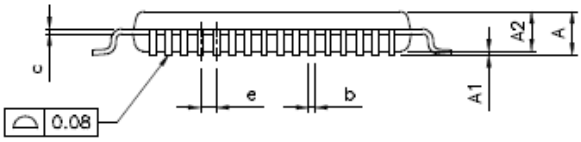
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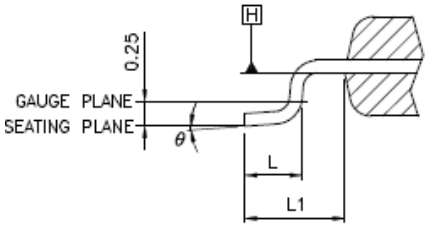
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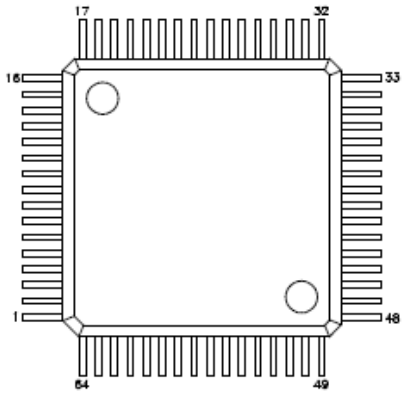


VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

SYMBOLS	MIN.	NOM.	MAX.
A	--	--	1.20
A1	0.05	--	0.15
A2	0.95	1.00	1.05
b	0.13	0.18	0.23
c	0.09	--	0.20
D	9.00 BSC		
D1	7.00 BSC		
E	9.00 BSC		
E1	7.00 BSC		
e	0.40 BSC		
L	0.45	0.60	0.75
L1	1.00 REF		
θ	0°	3.5°	7°







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12 Application Circuit

N/A

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